



2022 台灣靜電放電防護技術論壇--第二場 (CDM 靜電放電防護設計實例) 2022 Taiwan ESD Workshop (II) -- (On-Chip CDM ESD Protection Design)

活動內容

時間(Time)	課程 (Course Agenda)
13:00-13:30	Registration
13:30-14:50	Stacking-MOS Protection Design for Interface Circuits against Cross-Domain CDM ESD Stresses Speaker: Cheng-Yun Hsueh (薛承昀) <i>Phison Electronics CO., LTD</i>
14:50-15:10	Coffee Break
15:10-16:30	Study of CDM ESD Robustness among On-Chip Decoupling Capacitors in CMOS Integrated Circuits Speaker: Yi-Chun Huang (黃逸君) <i>National Yang Ming Chiao Tung University</i>
16:30-17:00	Q&A

時間與地點

2022 年 2 月 16 日 (三)

國立陽明交通大學光復校區交映樓 1F 國際會議廳

主辦單位

- (1) 積體電路與電子系統之靜電放電防護技術產學聯盟 (ESD 產學聯盟)
<http://www.alab.ee.nctu.edu.tw/~esd/>
- (2) 台灣靜電放電防護工程學會 (Taiwan ESD Association, T-ESDA)
<http://t-esda.org/>

報名費用 (含當日講義)

1. T-ESDA 或 ESD 產學聯盟會員：NT\$ 1,000 元/人。
2. 非會員：NT\$ 1,500 元/人。
3. 學生：NT\$ 500 元/人。



課程摘要

Stacking-MOS Protection Design for Interface Circuits against Cross-Domain CDM ESD Stresses

Electrostatic discharge (ESD) is still a challenging reliability issue for integrated circuits (ICs) in advanced CMOS technology. With the development of ICs toward system-on-chip (SoC) applications, it has been common to integrate multiple separated power domains into a single chip for power management or noise isolation considerations. Besides, the fabricated transistors with thinner gate oxide for high-speed operation cause the ICs more sensitive to charged-device model (CDM) ESD events, especially under cross-domain stresses. The traditional cross-domain CDM ESD protection designs like local ESD clamp were used to mitigate overstress on interface, but may be suffered from power-up sequence and performance degradation. For better integration in chip-level design, interface circuits were should be optimized for higher area efficiency and CDM robustness. Thus, new protection schemes with stacking footer/header MOS structures and various gate connections were proposed and verified in 0.18- μm CMOS technology. In this work, proposed designs have been implemented at the transmitter (TX) and receiver (RX) module for validating higher ESD level under cross-domain CDM and HBM (Human Body Model) tests. Moreover, the impact of area, speed and power consumption between different structures was also investigated in detail. Finally, the CDM failure on the interface circuit was discovered by electrical and physical failure analysis. The de-layer SEM results presented the gate-oxide damage only in the receiver (RX) of the interface circuit after cross-domain CDM stresses.

Study of CDM ESD Robustness among On-Chip Decoupling Capacitors in CMOS Integrated Circuits

The integrated circuit (IC) products fabricated in the scaled-down CMOS processes with higher clock rate and lower power supply voltage (VDD) are more sensitive to the transient/switching noises on the power lines with the parasitic inductance induced by the bonding wire. The typical method to suppress the power line noise is to add on-chip decoupling capacitors. Meanwhile, electrostatic discharge (ESD) is also a challenging issue on IC reliability in advanced CMOS technology. For the ICs fabricated in an advanced process, with the thinner gate oxide, the circuits are particularly vulnerable to the charged-device model (CDM) ESD events. However, there was very limited research to investigate the ESD robustness on the decoupling capacitors, especially during the CDM ESD events. In this work, the CDM ESD robustness among different types of decoupling capacitors in ICs was investigated in a 0.18- μm CMOS technology.



線上報名網站

<http://www.alab.ee.nctu.edu.tw/~esd/TESDW/reg.html>

報名注意事項

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