Design Consideration for ESD and Latch-up

ESD and latch-up are two of the most frequent reliability issues for commercial IC's. They contribute more than 25% of total IC failure during manufacturing and in the field. While often overlooked in the design process, as other factors such as performance and cost always attract most of the attention, design for reliability eliminates major hurdle in product introduction. The presentation describes typical reliability requirement, testing, and qualification for commercial IC's and the ever-increasing challenge posed by advanced CMOS technology. Various approaches that are commonly adopted by industry to ensure ESD robustness and latch-up immunity will be discussed. The emphasis will be mainly for custom analog and RF IC application.

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