Chapter 1  CMOS Processing Flow

- 0.25um 1P5M
- 0.18um 1P6M
- 0.15um 1P7M
- 0.13um 1P8M
- 0.09um
- Copper Interconnection
- Mixed-Signal / RF
- CMOS Processing
- Processing Integration
# Characteristics of 0.25μm CMOS Logic Product

<table>
<thead>
<tr>
<th></th>
<th>CL025G</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Voltage</td>
<td>2.5 V</td>
</tr>
<tr>
<td>I/O Voltage Option</td>
<td>3.3 V or 5 V tolerant</td>
</tr>
<tr>
<td>Physical Gate</td>
<td>0.24-μm</td>
</tr>
</tbody>
</table>
| Contacted Metal Pitch | M1: 0.64-μm  
                         | M2~M4: 0.80-μm  
                         | M5: 0.90-μm         |
| Ring Oscillator Delay | 38 ps                                      |
| I_{OFF} Spec. (worst case) | 0.1 nA/μm                              |
| Well Formation   | Retrograde Well                             |
| Isolation        | Shallow Trench Isolation                    |
| Salicide         | TiSi2                                       |
| Metal            | Up to five layers AlCu                      |
| Via Fill         | Tungsten with CMP                           |
| Lithography      | Deep UV                                     |
## Characteristics of 0.18μm CMOS Logic Product Family

<table>
<thead>
<tr>
<th></th>
<th>CL018G</th>
<th>CL018LV</th>
<th>CL018LP</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Core Voltage</strong></td>
<td>1.8 V</td>
<td>1.5 V</td>
<td>1.8 V</td>
</tr>
<tr>
<td><strong>I/O Voltage Option</strong></td>
<td>3.3 V</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Physical Gate</strong></td>
<td>0.16-μm</td>
<td>0.13-μm</td>
<td>0.16-μm</td>
</tr>
<tr>
<td><strong>Contacted Metal Pitch</strong></td>
<td>M1: 0.46-μm</td>
<td>M2~M5: 0.56-μm</td>
<td>M6: 0.90-μm</td>
</tr>
<tr>
<td><strong>Ring Oscillator Delay</strong></td>
<td>28 ps</td>
<td>25 ps</td>
<td>36 ps</td>
</tr>
<tr>
<td><strong>I&lt;sub&gt;off&lt;/sub&gt; Spec. (worst case)</strong></td>
<td>0.1 nA/μm</td>
<td>1 nA/μm</td>
<td>0.003 nA/μm</td>
</tr>
<tr>
<td><strong>Well Formation</strong></td>
<td>Super-Steep Retrograde</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Isolation</strong></td>
<td>Shallow Trench Isolation</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Salicide</strong></td>
<td>CoSi&lt;sub&gt;2&lt;/sub&gt;</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Metal</strong></td>
<td>AlCu, up to six layers</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Via Fill</strong></td>
<td>Tungsten with CMP</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Lithography</strong></td>
<td>Deep UV, with Phase-Shift Mask</td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Applications</strong></td>
<td>Baseline e.g., ASIC</td>
<td>High Speed e.g., Graphics</td>
<td>Low Power e.g., Portables</td>
</tr>
</tbody>
</table>
### Characteristics of 0.15 μm CMOS Logic Product Family

<table>
<thead>
<tr>
<th></th>
<th>CL015LV</th>
<th>CL015G</th>
<th>CL015HS</th>
<th>CL015LP</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Core Voltage</strong></td>
<td>1.2 V</td>
<td>1.5 V</td>
<td>1.5 V</td>
<td>1.5 V</td>
</tr>
<tr>
<td><strong>I/O Voltage Option</strong></td>
<td>3.3 V</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Contacted Metal Pitch</strong></td>
<td>M1: 0.39-μm</td>
<td>M2-M6: 0.48-μm</td>
<td>M7: 0.90-μm</td>
<td></td>
</tr>
<tr>
<td><strong>Ring Oscillator Delay</strong></td>
<td>20 ps</td>
<td>23 ps</td>
<td>14 ps</td>
<td>31 ps</td>
</tr>
<tr>
<td><strong>I&lt;sub&gt;off&lt;/sub&gt; Spec. (worst case)</strong></td>
<td>&lt;1 nA/μm</td>
<td>&lt;1 nA/μm</td>
<td>17 nA/μm</td>
<td>&lt;0.005 nA/μm</td>
</tr>
<tr>
<td><strong>Well Formation</strong></td>
<td>Super-Steep Retrograde</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Isolation</strong></td>
<td>Shallow Trench Isolation</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Salicide</strong></td>
<td>CoSi2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Metal</strong></td>
<td>AlCu or Cu, up to seven layers</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Via Fill</strong></td>
<td>Tungsten or Copper, with CMP</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Lithography</strong></td>
<td>Deep UV, with phase-shifting mask</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Applications</strong></td>
<td>High-Performance e.g., Graphics</td>
<td>Core-Logic e.g., ASIC</td>
<td>Ultra-Fast e.g., CPU</td>
<td>Low-Power e.g., Portables</td>
</tr>
</tbody>
</table>
## Characteristics of 0.13 μm CMOS Logic Product Family

<table>
<thead>
<tr>
<th>Feature</th>
<th>CL013LV</th>
<th>CL013G</th>
<th>CL013HS+</th>
<th>CL013LP</th>
</tr>
</thead>
<tbody>
<tr>
<td>Core Voltage</td>
<td>1.0 V</td>
<td>1.2 V</td>
<td>1.2 V</td>
<td>1.5 V</td>
</tr>
<tr>
<td>I/O Voltage Option</td>
<td>3.3 V or 2.5 V</td>
<td>3.3 V or 2.5 V</td>
<td>3.3 V</td>
<td>3.3 V or 2.5 V</td>
</tr>
<tr>
<td>Contacted Metal Pitch</td>
<td>M1: 0.34-μm, M2~M7: 0.41-μm, M8: 0.90-μm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ring Oscillator Delay (ps/gate)</td>
<td>14 (std. Vt)</td>
<td>19 (std. Vt)</td>
<td>10 ps</td>
<td>28 ps</td>
</tr>
<tr>
<td></td>
<td>17 (high Vt)</td>
<td>27 (high Vt)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>15 (low Vt)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Ioff_nom Spec. (nA/μm)</td>
<td>10 (std. Vt)</td>
<td>0.3 (std. Vt)</td>
<td>15</td>
<td>0.0015</td>
</tr>
<tr>
<td></td>
<td>1 (high Vt)</td>
<td>0.03 (high Vt)</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>10 (low Vt)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Well Formation</td>
<td>Super-Sleep Retrograde</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Isolation</td>
<td>Shallow Trench Isolation</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Salicide</td>
<td>CoSi2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Metal</td>
<td>Copper interconnect up to eight layers</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Via Fill</td>
<td>Copper, with CMP</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Lithography</td>
<td>193/248 nm</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Applications</td>
<td>High-Performance e.g., Graphics</td>
<td>Core-Logic e.g., ASIC</td>
<td>Ultra-Fast e.g., CPU</td>
<td>Low-Power e.g., Portables</td>
</tr>
</tbody>
</table>
TSMC unveiled its full 90-nanometer technology under the brand name Nexsys and, at the same time announced that 90-nanometer risk production would start in September of 2002. Volume production of the Nexsys 90-nm process will be manufactured on 300mm wafers. Nexsys technology satisfies the power, performance and integration requirements of a broad spectrum of applications and includes high-performance, low-power, mixed-signal/RF, and embedded memory options. TSMC established the Nexsys brand for its next-generation SOC process technology platform. The company's 90-nm technology is the first TSMC process to adopt this brand. Nexsys offers a unique triple gate oxide option that facilitates three different oxide thicknesses on a single chip. The triple gate oxide feature removes design restrictions caused by various core/IO combination requirements and should lead to more innovative SOC designs. With 70-75% linear shrinkage and a two-times performance improvement, compared to TSMC's 0.13-micron technology, Nexsys is poised to become the de facto SoC process technology platform standard.
TSMC 0.09um

The 90-nm process technology features:
Core supply voltage ranging from 1.0V to 1.2V
I/O and analog blocks ranging from 1.8V to 3.3V
Multiple threshold voltage (Vt) option for optimized transistor speed and power consumption trade-offs
Extremely tight process control for 50-nanometer gate length - the high speed process
Ni-salicide for better sheet resistance (Rs) in narrow line widths
Nine-layer copper interconnect, with an extra redistribution layer optional for flip-chip package
Low-k dielectrics with k £ 2.9 for the lowest RC delay and power consumption
A fully logic process-compatible 90-nanometer version of the Nexsys mixed-signal/RF technology will be available in January 2003. Nexsys mixed signal/RF process will feature:
MiM capacitor
High resistance resistor
High Q inductor and varactor
DNW(deep N-well) bipolar junction transistor
TSMC 0.09um

TSMC has scheduled the release of embedded 1TRAMTM and 6T/8T SRAM by September 2002. A common 6T SRAM cell will be available in core, low-power and high-speed processes to enable SOC designs. Ultra-high-density (UHD) cell and high-cell-current (HC) cell for different applications will also be available at a later date. Aggressive release schedules of embedded 1TRAMTM and Flash make SOC designs on Nexsys more realistic than ever.

Launching Nexsys Prototyping Service
TSMC's will launch 90-nm prototyping service beginning in the second quarter of 2002. This cost-sharing prototyping service has become essential considering the escalating costs of masks and wafers for the 90-nm generation. The launching frequency will increase to every other month or more in 2003 to meet anticipated demand.
Copper Interconnection

The electrical resistance of copper interconnects is less than two-thirds that of tungsten-aluminum interconnects. The series resistance of copper via runs as low as 20% that of tungsten plugs. Starting from the 0.18-micron process, TSMC has offered customers the option of copper interconnects for the top two layers, which are commonly used for power, clock routing and bonding pads. With this option alone, customers can realize 15% RC delay reduction. TSMC provides both top two-layer and all-layer copper options at the 0.15-micron process. While copper offers the greatest performance advantage when implemented to the top two metal layers, TSMC also offers an all-layer copper option. In fact, TSMC’s 0.13-micron process and beyond will be built on an all copper interconnect architecture. The lower electrical resistance due to copper leads to improved power distribution and device performance throughout the chip. Copper also improves the electromigration resistance, a major concern in IC’s long term reliability, by as much as 50 times. Furthermore, copper’s lower resistance helps to reduce cross-talk by providing a better control over the tight metal pitch. In summary, advanced technology demands extremely high routing density that necessitates copper interconnects. TSMC made its commitment early and has successfully developed the industry-leading copper process.
Mixed Signal / RF

TSMC is the only dedicated foundry to offer all-CMOS mixed signal and RF 0.35-µm, 0.25-µm and 0.18-µm processes. The company's 0.35-µm process was recently used to manufacture the world's first fully integrated single-chip Bluetooth transceiver using all-CMOS 2.4GHz RF integrated circuit.

TSMC's CMOS Mixed Signal and RF processes provide designers with smaller device dimensions, increased performance and lower costs than expensive BiCMOS and gallium arsinide processes.
# Mixed Signal / RF

## Characteristics of TSMC MixedSignal/RF CMOS Family

<table>
<thead>
<tr>
<th></th>
<th>CM035</th>
<th>CM025</th>
<th>CM018</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Core Voltage</strong></td>
<td>3.3 V</td>
<td>2.5 V</td>
<td>1.8 V</td>
</tr>
<tr>
<td><strong>I/O Voltage Option</strong></td>
<td>3.3 or 5V</td>
<td>3.3 or 5V</td>
<td>3.3 V</td>
</tr>
<tr>
<td><strong>Physical Gate</strong></td>
<td>0.35-μm</td>
<td>0.24-μm</td>
<td>0.16-μm</td>
</tr>
<tr>
<td><strong>Metal</strong></td>
<td>Up to 4M+</td>
<td>Up to 5M+</td>
<td>Up to 6M+</td>
</tr>
<tr>
<td><strong>Contacted Metal Pitch</strong></td>
<td>M1: 0.95-μm, M2~M3: 1.10-μm, M4: 1.20-μm</td>
<td>M1: 0.64-μm, M2~M4: 0.80-μm, M5: 0.90-μm</td>
<td>M1: 0.46-μm, M2~M5: 0.56-μm, M6: 0.90-μm</td>
</tr>
<tr>
<td><strong>Ring Oscillator Delay</strong></td>
<td>51 ps</td>
<td>38 ps</td>
<td>28 ps</td>
</tr>
<tr>
<td><strong>I\text{OFF} Spec. (worst case)</strong></td>
<td>0.1 nA/μm</td>
<td>0.1 nA/μm</td>
<td>0.01 nA/μm</td>
</tr>
<tr>
<td><strong>Well Formation</strong></td>
<td>Twin well (drive in)</td>
<td>Retrograde well</td>
<td>Super Steep retrograde</td>
</tr>
<tr>
<td><strong>Isolation</strong></td>
<td>LOCOS</td>
<td>STI(shallow trench isolation)</td>
<td>STI</td>
</tr>
<tr>
<td><strong>Salicide</strong></td>
<td>TiSi₂</td>
<td>TiSi₂</td>
<td></td>
</tr>
<tr>
<td><strong>Capacitor</strong></td>
<td>Metal(MiM) or Poly(PiP)</td>
<td>Metal(MiM) or Poly(PiP)</td>
<td>MiM</td>
</tr>
<tr>
<td><strong>Inductor</strong></td>
<td>Thick Metal(Top)</td>
<td>Thick Metal(Top)</td>
<td>Thick Metal(Top)</td>
</tr>
<tr>
<td><strong>Via Fill</strong></td>
<td>W plug</td>
<td>W plug</td>
<td>W plug</td>
</tr>
<tr>
<td><strong>Lithography</strong></td>
<td>I-line</td>
<td>Deep UV</td>
<td>Deep UV(phase shift mask)</td>
</tr>
</tbody>
</table>
**CMOS PROCESSING**

**Silicon Wafer**

*Czochralski method* – single-crystal method

- starts with a seed of single crystal silicon, and the pull rate and speed of rotation determine the diameter of the crystal rod or ingot
- heavily doped silicon is added to the melt before the single-crystal ingot is pulled
- the ingot is cut into wafers using a large diamond saw
- $p^-$ is doped around $N_A \equiv 2 \times 10^{21}$ donor/m$^3$, *resistivity* $\equiv 10$-20 $\Omega \cdot$ cm.
Epitaxial

The surface of wafer might be doped more heavily, and a single-crystal epitaxial layer of the opposite type might be grown over its surface.
Photolithography

Selected portion of silicon wafer can masked out so that the some type of processing step can be applied to the remaining areas.

- grow a thin oxide (SiO$_2$) to protect the surface
Photoresist

- **negative photoresist**, exposed photoresist remains after the masking
- **positive photoresist**, exposed photoresist is dissolved by organic solvents, the photoresist still remains where the mask was opaque
- By using both positive and negative photoresist, a single mask can sometimes be used for two steps.
Diffusion

Forming an n well by diffusing phosphorus from a gas into the silicon, through the opening in the SiO₂
- Dopant is Phosphorus for n-well, Arsenic takes much longer time to diffuse.
- 900-1100 °C, high temperature causes dopant to diffuse vertically and laterally. Dopant concentration is the greatest at surface.
- **Boron** for p-well.
Ion implementation

An ion-implantation system
- Allows more independent control over concentration and the thickness of doped region.
- Ion beams are focused and accelerated at 10 keV and 1 MeV.
- Lattice damage due to nuclear collisions results in displacement of substrate atoms.
- Narrow profile results in heavy concentration (Arsenic with 100 keV, 0.06 um ± 0.02 um).
- Greater control over doping level.
- Much smaller side wall diffusion, allows devices to be more closely spaced, minimize overlap between gate-source and gate-drain regions.
Annealing

Dopant profiles after ion implantation both before and after annealing
- 1000 °C for 15-30 minutes, then cooled down.
- Broaden concentration profile, make profile more uniform.
- Solve the above mentioned problems in ion implementation.
Chemical Vapor Deposition

- E.g. $\text{Si}_3\text{N}_4$ deposited during a gas-phase reaction at about 800 °C.

Field-implementation

The cross section when field-implants are being formed
- Field implant where field-oxide grown.
- Guarantee silicon under field-oxide will never invert when the conductor over the field-oxide has a large voltage.
- Leakage between junctions of separate transistors in the substrate region is intended to be unconnected.
Growing Field-Oxide: *thermal oxide*

**Wet process:** water vapor diffuses into silicon

\[ \text{Si} + 2\text{H}_2\text{O} \rightarrow \text{SiO}_2 + 2\text{H}_2 \]

**Dry process:** oxygen introduced over wafer, slightly higher temperature then wet process

\[ \text{Si} + \text{O}_2 \rightarrow \text{SiO}_2 \]

The cross section after the field-oxide has been grown.
- SiO₂ takes up approximately 2.2 times the volume of the original silicon, causes SiO₂ to extend approximately 45 percent into, and 55 percent above the surface.
- Wet process is faster because H₂O diffuses faster in silicon than O₂ does.
- Dry process results in denser, higher-quality SiO₂ that is less porous.
Gate-Oxide and Threshold-Voltage Adjust

Cross section after the thin gate-oxide growth and threshold-adjust implant.
- After gate-oxide (about < 0.01-0.03 um) is grown, donors (boron) are implemented through the oxide to adjust the threshold voltage.
- p-transistor and n-transistor are adjusted at the same time (n-transistor from -0.1 to 0.7-0.8, p-transistor from -1.6 to -0.8-0.9).
- Higher doping level increases the junction capacitance and body effect of transistors in the well.
- Double threshold adjust allows optimum well doping.
Polysilicon Gate Formation

Cross section after depositing and patterning the polysilicon gates.

- Chemical deposition of polysilicon with silane (SiH$_4$) gas.
- 650 °C, noncrystalline or amorphous. (1000-1250 °C on silicon to create single-crystal silicon)
- Ion implanted with Arsenic to increase its conductivity (10-30 Ω/□)
Implanting Junction

Cross section after ion-implanting the p⁺ junctions.
Cross section after ion-implanting the n⁺ junctions.
- Boron implemented to from p+ region. self-aligned to poly edge, resulting in very little overlap.
- p+ also for substrate Vss contact to prevent latch-up.
- Arsenic implemented to from n+ region.
- N+ also for n-well \( V_{DD} \) contact to prevent latch-up.
- After all junctions have been implanted, the complete wafer is covered in CVD SiO\(_2\). 500 °C, 0.25-0.5 um.
- Next step, open contact hole.
 Depositing and Patterning Metal

- Aluminum (Al) for interconnection
- *Evaporation* techniques in a vacuum, the heat for evaporation is produced by electron-beam bombarding in a sputtering system.
- Low-temperature annealing (550°C), give better bonds between metal and silicon.
Overglass Deposition

Final *passivation* CVD SiO$_2$ is deposited, often an additional Si$_3$N$_4$ is deposited for better impervious to moisture.

Final cross section of an example CMOS microcircuit.
Some possible process:

- twin wells
- poly-poly capacitor, thin thermal oxide
- high resistivity poly, 1G $\Omega/\square$, SRAM
- field-implant under field-oxide in well region
- n-channel and p-channel transistors with different threshold adjust
- 2, 3, 4, 5, or 6 layer of metal
- planarized after each metal-patterning step, reactive etching, cover with SiO$_2$, the hills are etched faster than the valleys
- thin-film nichrome resistors under the top layer of metal
- transistors realized in epitaxial layer
- BiCMOS
Bipolar Processing

Cross section of a modern, self-aligned bipolar transistor with oxide isolation. The term “poly” refers to polysilicon
- **p**⁻ substrate
- **n**⁺ region to lower series collector resistance
- **n**⁻ *single-crystal* epitaxial
- **n**⁺ collector contact region is implemented, the region extends from surface down to **n**⁺ buried region
- polysilicon is used to contact emitter, base, collector
- base **p**⁺ polysilicon is deposited first, during a high temperature step, the boron dopant from polysilicon contact diffuses into silicon to make underlying region **p**⁺.
- base polysilicon is covered with a thin layer of SiO₂ (0.5um in thickness), the SiO₂ spacer allows the base contact, thereby minimizing base resistance.
- **n**⁺ from emitter polysilicon diffuses into the base **p** silicon to from emitter region.
PROCESSING INTEGRATION
N-WELL CMOS TECHNOLOGY

(a)
Figure 1: Well implant and drive-in in the n-well CMOS inverter. Window in the mask (a) and cross-section (b)
(a) field oxide
Figure 2: Formation of the active regions in the n-well CMOS inverter. Window in the mask (a) and cross-section of the inverter (b).
(a)
**Figure 3:** Active regions in the n-well CMOS inverter. Edges of active regions in the mask (a) and cross-section of the inverter.
Figure 4: Gate oxide growth in the n-well CMOS inverter. Edges of the gate oxide regions (a) and cross-section of the inverter (b).
CVD: usually doped with n-type impurity with low resistivity
Figure 5: Polysilicon region in the n-well CMOS inverter. Window in the mask (a) and cross-section of the inverter (b).
Figure 6: Implantation of n-channel transistor drain and source. Window in the n-select mask (a) and cross-section of the inverter (b).
Figure 7: Implantation of $p^+$ regions. Window in the negative of the n-select mask (a) and cross-section of the inverter (b).
Source/drain annealing at a shoot thermal process to repair some of the crystal structure change occur in the high-close implantation without significant lateral diffusion.

Figure 8: N+ region in the n-well of the CMOS inverter. Edges of the drain region of the p-channel device and the n+ region in the n-well (a) and cross-section of the inverter (b).
Figure 9: CVD deposition of SiO$_2$ in the n-well CMOS process. Layout (a) and cross-section of the inverter (b)

The nonplanarity of the surface will have an impact on the metal deposition step.
- in the source/drain areas or poly layers.
- contacts to poly must be made outside the gate region to avoid metal spikes through the poly and the thin gate oxide.

(a)
Figure 10: Contact cuts in the n-well CMOS inverter. Window in the mask (a) and cross-section of the inverter (b).
- "Al" deposited over the entries wafer
- Step coverage is the most critical.
- undefined Al is removed.
Figure 11: Metallization in the n–well CMOS inverter. Window in the mask (a) and cross-section of the inverter (b).
Final step: passivation glass to protect the surface from contaminants and scratches.

(a)
(b)
Figure 12: CMOS inverter. Composite layout (a), cross-section (b), and electrical diagram (c).
LDD allow very small transistor without suffering from "hot electron"

(a)

(b)
(c) 

(d) 

low temperature oxide 

LTO SiO₂
Figure 13: Formation of the LDD transistor structure
TWIN-Well CMOS PROCESS

twin-well
- allows independent control of the threshold voltage.
- keeps resistivity of the wells small.

(a)
(b) 

![Diagram of SiO₂ layer with n⁻ and p⁺ regions.]

(c) 

![Diagram with n⁻ and p⁺ regions.]
(d) 

Photoresist

(e) 

Si$_3$N$_4$
Figure 14: Advanced CMOS process. Part 1.

during the steps, both P-well and n-well are rediffused deeper.
Figure 15: Advanced CMOS process. Part 2.
due to the large diffusivity of Boron, the edge of the p-channel are moving jauter than the edges of the n-transistor

Figure 16: Advanced CMOS process. Part 3.
first metal

or Alloys of Al, Mo, and W
Figure 17: Advanced CMOS process. Part 4.

the surface has to be planarized before deposition of another layer

Photoresist
etched with a solution that has the same etching rate for photoresistor & oxide

(a)
Figure 18: Advanced CMOS process. Part 5.
- two layer method, high quality due to planarization step
- LDD:NMOS preventing hot-electron phenomena
- optimal threshold voltage both PMOS & NMOS through twin-well
- good latch-up protection by minimizing, the lateral voltage drops inside the wells
Figure 19: Summary of basic features.
Chapter 2 Layout Design Rules

- Layout Design Rules
- Definition of Layout Rules
- Stick Diagram
- Euler Path
- CMOS Inverter Layout
Layout Design Rules

- a prescription for preparing the photomasks that are used in the fabrication of integrated circuits.
- a set of specification for the mask patterns used in the layout and provide geometry information such as the minimum width and spacing for each layer.
- provide a necessary communication link between circuit designer and process engineer during the manufacturing phase.
- obtain the circuit with option yield in an small a geometry as possible without compromising reliability of the circuit.
Layout Design Rules

- Compromise between performance and yield

  - the more conservative the rules are, the most likely it is that the circuit will function.
  - the more aggressive the rules are, the greater the probability of improvements in circuit performance, this improvement may be at the expense of yield.

The design rules primarily address two issues:

1. The geometrical reproduction of features that can be reproduced by the mask masking and lithography process.
2. The interaction between different layers.
Physical Basic of Design Rules

- limitation of lithography
- physics of the process flow
- electrical characteristics of the final structure

Minimum line width

- limitation on the lithographic resolving power.
- if the line width are made too small, it is possible for the to be discontinuous.
Minimum Spacing

- Lines on a given layer also tend to originate form the lithography.
- If the wire are placed two close, it is possible for them to merge together.
- Lines on different layers: restriction arises because the layers must be stacked to form devices.
- Spacing between lines of different layers are chosen to compensate for misalignment or registration errors in the layering process, thus a registration tolerance must be allowed.
Active Area Definition in a LOCOS Process

- active area encroachment induced by the formation of the bird’s beak requires that the nitride mask dimensions be larger than the final active area.

Poly gate overhang distance

- ensure that the source/drain region will be separated in the event of a misalignment between the active area and the poly mask.
Implant in a Depletion-Mode MOSFET

- The implanted region must be larger than the device active area to ensure that misalignment does not occur.

Well rules
Well Rules

- The well is usually a deeper implant compared with the transistor source/drain implant, therefore it is necessary for the outside dimension to provide sufficient clearance between the n-well and the adjacent different region.
- The inside clearance is determined by the transition of the yield oxide across the well boundary, "bird’s beak" effect.
- To avoid shorten condition, active region is not permitted to cross a well boundary.
- Sheet resistance of well is about several kΩ/□, it is necessary thoroughly contact the well to VDD or VSS, this will prevent excessive voltage drops due to substrate current.
Transistor Rules

- where poly crosses active, the source and drain diffusion is masked by the region, the source, drain, and channel are therefore self-aligned to the gate.

- poly is necessary to extend beyond the edges of the diffusion region to the drain and source will not be shorted.

- poly and active region that do not meet intentionally to form a transistor should be kept separated.

- two of implant/diffusion layers to form the p- and n-transistor.
Contact Rules

- metal to p-active (p-diffusion)
- metal to n-active (n-diffusion)
- metal to polysilicon
- VDD and VSS substrate contacts
- split (substrate constant)

- depending on process, “buried contact” (poly-diffusion) maybe allowed. Ex: NMOS process, SRAM process.
- each isolated well must be tied to the appropriate supply voltage.
- the split or merge (butting) contact is equivalent to two separate metal-diffusion contacts that are strapped together with metal.
Layout Design Rules

Guard Ring

p+ diffusion in the p-substrate (p-well) and n+ diffusion in the n-well are used to collect injected minority carriers. n+ guard rings tied to VDD. p+ guard rings tied to VSS.
Metal1 rules

- metal spacing may vary with the width of the metal line (so-called fat-metal rules), this is due to etch characteristics of small versus large metal wires.
- some process require a certain proportion of the chip area to be covered with metal.

Via rules

- process may vary in whether they allow via to be placed over poly and diffusion.
- some process allow via to be placed within these areas but not allow the via to straddle the boundary of poly or diffusion, this results from the sudden vertical topology variations that occur at sublayer boundaries.
Metal2 rules

- the possible increase in width and separation of 2\textsuperscript{nd} level metal are conservative rules to ensure against broken conductor or shorts between adjoining wire due to vertical topology.
- modern processes frequency have the metal1 and metal2 pitches identical.

Via2 rules

- similar to 1st via, the rules for placement of via2 may vary with process.

Metal3 rules

- the rules usually but not always increase in width and separation over metal2.
- metal3 is generally need primarily for power-supply connections and clock distribution.
Passivation or overglass

- this is a protective glass layer that covers the final chip, opening are required at pads and any internal test points.

Definition of the layout layers
“Line of Diffusion” Rule

- The transistors from a line of diffusion intersected by polisilicon gate connections.
- The CMOS circuit is converted to a graph where
  1. The vertices in the graph are the source/drain connections.
  2. The edges in the graph are transistors that connect particular source-drain vertices.
- Two graphs, one for the n-logic tree and one for the p-logic tree result.
- The connection of edges in the graph mirror the series-parallel connection of gate signal name for that particular transistor.
N-Well
Cross-Sectional & Layout View

- PW mask is a reverse tone of N-Well mask without bias.

<table>
<thead>
<tr>
<th>Rule No.</th>
<th>Description</th>
<th>Layout Rule</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer</td>
<td>NW --- N-Well</td>
<td></td>
</tr>
<tr>
<td>NW.W.1</td>
<td>Min. dimension of a NW region</td>
<td>A ( \mu \text{m} )</td>
</tr>
<tr>
<td>NW.S.1</td>
<td>Min. space between two NW regions with the same potential</td>
<td>B ( \mu \text{m} )</td>
</tr>
<tr>
<td>NW.S.2</td>
<td>Min. space between two NW regions with different potential</td>
<td>C ( \mu \text{m} )</td>
</tr>
</tbody>
</table>
# Thin Oxide Cross-Sectional & Layout View

![Diagram of Thin Oxide Cross-Sectional & Layout View](image)

## Thin Oxide Definition

<table>
<thead>
<tr>
<th>Rule No.</th>
<th>Description</th>
<th>Layout Rule</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer:</td>
<td>OD --- Thin Oxide Definition</td>
<td></td>
</tr>
<tr>
<td>OD.W.1</td>
<td>Mini. width of an OD region</td>
<td>A</td>
</tr>
<tr>
<td>OD.S.1</td>
<td>Mini. space between two OD regions</td>
<td>B</td>
</tr>
<tr>
<td>OD.C.1</td>
<td>Mini. clearance from NW edge to a N+ OD region which is inside the NW</td>
<td>C</td>
</tr>
<tr>
<td>OD.C.2</td>
<td>Mini. clearance from NW edge to a N+ OD region which is outside the NW</td>
<td>D</td>
</tr>
<tr>
<td>OD.C.3</td>
<td>Mini. clearance from NW edge to a P+ OD region which is inside the NW</td>
<td>E</td>
</tr>
<tr>
<td>OD.C.4</td>
<td>Mini. clearance from NW edge to a P+ OD region which is outside the NW</td>
<td>F</td>
</tr>
</tbody>
</table>
Ploy
Cross-Sectional & Layout View

Rule No. | Description                                                                 | Layout Rule
---------|-----------------------------------------------------------------------------|------------
Layer :  | PO --- Poly Si                                                              |            |
PO.W.1   | Min. width of a PO region for the channel length                           | A          | um        |
PO.S.1   | Min. space between two PO regions on OD area                               | B          | um        |
PO.O.1   | Min. overlap of a PO region extended into field oxide (endcap)             | C          | um        |
P.O.C.1  | Min. clearance from a PO gate to a related OD edge                         | D          | um        |
P+ Implant
Cross-Sectional & Layout View

<table>
<thead>
<tr>
<th>Rule No.</th>
<th>Description</th>
<th>Layout Rule</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer</td>
<td>PP → P+ Implantation</td>
<td></td>
</tr>
<tr>
<td>PP.W.1</td>
<td>Min. width of a PP region</td>
<td>A um</td>
</tr>
<tr>
<td>PP.S.1</td>
<td>Min. space between two PP regions</td>
<td>B um</td>
</tr>
<tr>
<td>PP.E.1</td>
<td>Min. extension of a PP region beyond a PP active OD region</td>
<td>C um</td>
</tr>
</tbody>
</table>
N+ Implant
Cross-Sectional & Layout View

<table>
<thead>
<tr>
<th>Rule No.</th>
<th>Description</th>
<th>Layout Rule</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer:</td>
<td>NP --- N+ Implantation</td>
<td></td>
</tr>
<tr>
<td>NP.W.1</td>
<td>Min. width of a NP region</td>
<td>A  um</td>
</tr>
<tr>
<td>NP.S.1</td>
<td>Min. space between two NP regions</td>
<td>B  um</td>
</tr>
<tr>
<td>NP.E.1</td>
<td>Min. extension of a NP region beyond a NP active OD region</td>
<td>C  um</td>
</tr>
<tr>
<td>NP.C.1</td>
<td>Min. clearance between PP and NP</td>
<td></td>
</tr>
</tbody>
</table>

* PP and NP implant have to cover all poly to reduce the resistance
## Contact Cross-Sectional & Layout View

![Cross-Sectional & Layout View](image)

### Rule No. Description

<table>
<thead>
<tr>
<th>Rule No.</th>
<th>Description</th>
<th>Layout Rule</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer</td>
<td>CO --- Contact Window</td>
<td></td>
</tr>
<tr>
<td>CO.W.1</td>
<td>Min. and max. width of an CO region</td>
<td>A um</td>
</tr>
<tr>
<td>CO.S.1</td>
<td>Min. space between two CO regions</td>
<td>B um</td>
</tr>
<tr>
<td>CO.C.1</td>
<td>Min. clearance from a CO on OD region to a PO gate</td>
<td>C um</td>
</tr>
<tr>
<td>CO.C.2</td>
<td>Min. clearance from a CO on PO region to an OD region</td>
<td>D um</td>
</tr>
<tr>
<td>CO.E.1</td>
<td>Min. extension of an OD region beyond a OD CO region</td>
<td>E um</td>
</tr>
<tr>
<td>CO.E.2</td>
<td>Min. extension of a PO region beyond a Poly CO region</td>
<td>F um</td>
</tr>
</tbody>
</table>
Metal-1
Cross-Sectional & Layout View

<table>
<thead>
<tr>
<th>Rule No.</th>
<th>Description</th>
<th>Layout Rule</th>
</tr>
</thead>
<tbody>
<tr>
<td>Layer:</td>
<td>M1 --- Metal-1</td>
<td></td>
</tr>
<tr>
<td>M1.W.1</td>
<td>Minimum width of M1 region</td>
<td>A um</td>
</tr>
<tr>
<td>M1.S.1</td>
<td>Minimum space between two M1 regions</td>
<td>E um</td>
</tr>
<tr>
<td>M1.E.1</td>
<td>Minimum extension of M1 region beyond CO region</td>
<td>C um</td>
</tr>
<tr>
<td>M1.E.2</td>
<td>Minimum extension of M1 end-of-line region beyond CO region</td>
<td>C um</td>
</tr>
<tr>
<td>M1.S.2</td>
<td>Minimum space between metal lines with one or both metal line width and length are greater than 10um</td>
<td>E um</td>
</tr>
<tr>
<td>M1.A.1</td>
<td>Minimum area of M1 region</td>
<td>E um²</td>
</tr>
<tr>
<td>M1.R.1</td>
<td>Minimum density of M1 area</td>
<td></td>
</tr>
</tbody>
</table>

* Density is calculated as Total metal layout area/chip area
Via1
Cross-Sectional & Layout View

Rule No. | Description                                                                 | Layout Rule |
---------|-----------------------------------------------------------------------------|-------------|
Layer :  | VIA1 --- Via1 Hole                                                           |             |
VIA1.W.1 | Min. and max. width of VIA1 region                                           | A um        |
VIA1.S.1 | Minimum space between two VIA1 regions                                       | B um        |
VIA1.E.1 | Minimum extension of M1 region beyond VIA1 region                           | C um        |
VIA1.E.2 | Minimum extension of M1 end-of-line region beyond VIA1 region               | D um        |
VIA1.C.1 | VIA1 can be fully or partially stacked on CO                                 |             |
Metal-2
Cross-Sectional & Layout View

Rule No. | Description | Layout Rule
--- | --- | ---
Layer : | M2 --- Metal-2 |  
M2.W.1 | Minimum width of M2 region | A | um  
M2.S.1 | Minimum space between two M2 regions | B | um  
M2.E.1 | Minimum extension of M2 region beyond VIA1 region | C | um  
M2.E.2 | Minimum extension of M2 end-of-line region beyond VIA1 region | D | um  
M2.A.1 | Minimum area of M2 region | E | um²  
M2.R.1 | Minimum density of M2 area | \( \text{Density} = \frac{\text{Total metal layout area}}{\text{chip area}} \)
## Technology Parameters for Typical Case

### TECHNOLOGY PARAMETERS FOR TYPICAL CASE:

#### Conductor layers

<table>
<thead>
<tr>
<th>Conductor</th>
<th>Thickness</th>
<th>Min. width</th>
<th>Min. space</th>
<th>Distance between conductor layer and substrate under FOX</th>
</tr>
</thead>
<tbody>
<tr>
<td>PO1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M1</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M2</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M3</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M4</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M5</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

#### Dielectric layers

<table>
<thead>
<tr>
<th>Dielectric</th>
<th>Thickness</th>
<th>Dielectric constant</th>
<th>Comment</th>
</tr>
</thead>
<tbody>
<tr>
<td>FOX</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ILD</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IMD1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IMD2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IMD3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>IMD4</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PASS1</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>PASS2</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
DNW (deep N-Well definition)

Cross section (X-X) for NW, RW, and DNW
Seal Ring Rule
Chapter 3  Analog Layout Consideration

- Failure Mechanism
- Matching Issues
- Design for Low Offset and Drift
- Matching Capacitors
- Matching Resistors
Histogram of the mismatch, $\delta$, of 30 units, showing mean, $m_\delta$, and standard deviation, $s_\delta$. 
Matching Issues

- lateral diffusion
- etching under protection
- boundary dependent etching
- three dimensional effects
- errors and limitations associated with mask production and mask alignment
- the effects must be avoided or compensated
Matching Issues

(a) Lateral diffusion; (b) etching under the protection; (c) boundary dependent etching.
Matching Issues

Various two-dimensional effects causing sizes of realized microcircuit components to differ from sizes of layout masks. Error in the pattern size due to tri-dimensional effects.
Design for Low Offset and Drift

- global performance of analog circuit is strongly dependent on absolute and relative accuracy of basic component
- accuracy depends on relevant properties of materials and geometry of components
- absolute accuracy can be controlled at technology level
- relative inaccuracy, due to gradients and local variation, controlled at technology level, can be compensated with suitable layout techniques
- parameters depend on different technology steps, assume to be statistically independent, by summing up various error contribution
- use dimensions larger than ones indicated to have inaccuracy not dominated by geometry parameters
- distance of matched elements increases matching accuracy worsens
Design for Low Offset and Drift

- compensate gradient effects with *interdigitized* and *common centroid* layout
- matched devices operated at same temperature, realign to same *isothermal*
- *increasing sizes* of devices for better matching
- *minimum distance* from each other
- layout devices with same orientation with respect to silicon crystal, putting them in parallel, current tack same direction (MOS has different mobility in different orientation)
- same area to perimeter ration
- easier to match round devices than square devices, the number of bends and corners in the connection between pairs must be the same
Identification of directions on (100) and (111) wafers.
Coefficients of thermal expansion (CTE) for several materials used in packaging integrated circuits.

<table>
<thead>
<tr>
<th>Material</th>
<th>CTE ppm / °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Epoxy encapsulation</td>
<td>24</td>
</tr>
<tr>
<td>Copper alloys</td>
<td>16~18</td>
</tr>
<tr>
<td>Alloy-42</td>
<td>4.5</td>
</tr>
<tr>
<td>Molybdenum</td>
<td>2.5</td>
</tr>
<tr>
<td>Silicon</td>
<td>2.5</td>
</tr>
</tbody>
</table>
Chip Layout with Isotherms

- Isotherms
- Differential pairs
- Good
- Bad
- Power devices
Boundary Condition

Boundary dependent etching.

Compensation of Boundary dependent etching with dummy elements.
Current Oriented Match

![Diagram showing current oriented match with labels Idd, M1, M2, and examples of normal and better orientations.]
Dummy Layout for Capacitor

dummy

poor

better
Many contacts, with minimum spacing, lead to reduced curvature of the surface of the metal, thus reducing the risk of micro-fractures (potential source of failure) in the body of the metal connections.
Random Mismatches due to Microscopic Variations
Weight Current Cell Layout

The same boundary condition

\[
\frac{W - \Delta W}{L - \Delta L} \quad \frac{2W - \Delta W}{2L - \Delta L} \quad \frac{4W - \Delta W}{4L - \Delta L}
\]

(Wrong)

\[
\frac{W - \Delta W}{L - \Delta L} \left( \frac{W - \Delta W}{L - \Delta L} \right) \times 2 \quad \frac{W - \Delta W}{L - \Delta L} \times 4
\]

(Right)
Locating (a) the centroids of a rectangle and (b) dogbone resistor.

Examples of one-dimensional common-centroid arrays.
Sample interdigitation patterns for arrays having one axis of symmetry.

<table>
<thead>
<tr>
<th>A</th>
<th>AA</th>
<th>AAA</th>
<th>AAAA</th>
</tr>
</thead>
<tbody>
<tr>
<td>AB*</td>
<td>ABBA</td>
<td>ABBAAB*</td>
<td>ABABBABA</td>
</tr>
<tr>
<td>ABC*</td>
<td>ABCCBA</td>
<td>ABCBACBCA*</td>
<td>ABCABCCBACBA</td>
</tr>
<tr>
<td>ABCD*</td>
<td>ABCDDCBA</td>
<td>ABCDBCADBDA*</td>
<td>ABCDDCBAABCDDCBA</td>
</tr>
<tr>
<td>ABA</td>
<td>ABAABA</td>
<td>ABAABAAB</td>
<td>ABAABAABABA</td>
</tr>
<tr>
<td>AABABA</td>
<td>AABABAABABA</td>
<td>AABABAABABA</td>
<td>AABABAABABAABCABABA</td>
</tr>
<tr>
<td>AABA*</td>
<td>AABAABA</td>
<td>AABAABAABABA*</td>
<td>AABAABAABABAABAA</td>
</tr>
<tr>
<td>AABAA</td>
<td>AABAAAAABAA</td>
<td>AABAAAAABAAAAABAA</td>
<td>AABAAAAABAAAAABAAAAABAA</td>
</tr>
</tbody>
</table>
The four rules of common-centroid layout.

<table>
<thead>
<tr>
<th><strong>1. Coincidence:</strong></th>
<th>The centroids of the matched devices should coincide at least approximately. Ideally, the centroids should exactly coincide.</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>2. Symmetry:</strong></td>
<td>The array should be symmetric around both the X- and Y-axes. Ideally, this symmetry should arise from the placement of segments in the array and not from the symmetry of the individual segments.</td>
</tr>
<tr>
<td><strong>3. Dispersion:</strong></td>
<td>The array should exhibit the highest possible degree of dispersion; in other words, the segments of each device should be distributed throughout the array as uniformly as possible.</td>
</tr>
<tr>
<td><strong>4. Compactness:</strong></td>
<td>The array should be compact as possible. Ideally, it should be nearly square.</td>
</tr>
</tbody>
</table>

Hong-Yi Huang 黃弘一
Examples of two dimensional common centroid arrays.
Sample interdigitation patterns for two-dimensional common-centroid arrays.

<table>
<thead>
<tr>
<th>ABB</th>
<th>ABB</th>
<th>ABB</th>
<th>ABB</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABB</td>
<td>ABA</td>
<td>ABB</td>
<td>ABB</td>
</tr>
<tr>
<td>BAA</td>
<td>ABA</td>
<td>ABA</td>
<td>ABA</td>
</tr>
<tr>
<td>BA</td>
<td>BAA</td>
<td>BAA</td>
<td>BAA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ABA</th>
<th>ABA</th>
<th>ABA</th>
<th>ABA</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABA</td>
<td>ABA</td>
<td>ABA</td>
<td>ABA</td>
</tr>
<tr>
<td>BAB</td>
<td>BAB</td>
<td>BAB</td>
<td>BAB</td>
</tr>
<tr>
<td>BAB</td>
<td>BAB</td>
<td>BAB</td>
<td>BAB</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>ABC</th>
<th>ABC</th>
<th>ABC</th>
<th>ABC</th>
</tr>
</thead>
<tbody>
<tr>
<td>ABC</td>
<td>ABC</td>
<td>ABC</td>
<td>ABC</td>
</tr>
<tr>
<td>CBA</td>
<td>CBA</td>
<td>CBA</td>
<td>CBA</td>
</tr>
<tr>
<td>CBA</td>
<td>CBA</td>
<td>CBA</td>
<td>CBA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>AAB</th>
<th>ABA</th>
<th>ABA</th>
<th>ABA</th>
</tr>
</thead>
<tbody>
<tr>
<td>AAB</td>
<td>ABA</td>
<td>ABA</td>
<td>ABA</td>
</tr>
<tr>
<td>BAA</td>
<td>BAA</td>
<td>BAA</td>
<td>BAA</td>
</tr>
<tr>
<td>BAA</td>
<td>BAA</td>
<td>BAA</td>
<td>BAA</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>AAB</th>
<th>ABA</th>
<th>ABA</th>
<th>ABA</th>
</tr>
</thead>
<tbody>
<tr>
<td>AAB</td>
<td>ABA</td>
<td>ABA</td>
<td>ABA</td>
</tr>
<tr>
<td>BAA</td>
<td>BAA</td>
<td>BAA</td>
<td>BAA</td>
</tr>
<tr>
<td>BAA</td>
<td>BAA</td>
<td>BAA</td>
<td>BAA</td>
</tr>
</tbody>
</table>
Failure Mechanisms

ESD – electrostatic discharge

Representative ESD tests: 2kV human body model (a) and 200V machine model (b) In both circuits, DUT stands for device under test.
Electromigration

The antenna Effect

A layout susceptible to the antenna effect (a) can be made immune by the addition of a metal jumper (b)
Contamination

Dry Corrosion

Mobile Ion Contamination

Behavior of mobile ions under bias: ions that were randomly distributed through the oxide (a) shift in unison in response to a positive gate bias (b)
Scribe Seals

Scribe seals for single- and double-level-metal variants of a CMOS or BiCMOS process. Depending on the manufacturer, various diffusions may also be placed over the scribe street.
A weak electric field causes an overall drift of carriers but does not materially affect their instantaneous velocity (a), while a strong electric field actually increases the instantaneous velocity of the carriers.
Hot Carrier Injection

Simplified diagram showing the mechanism responsible for hot electron injection in an NMOS transistor.
Zener Walkout Mechanism

Simplified diagram showing Zener walkout mechanism: (a) initial condition of junction, in which hot carrier production occurs near the surface; (b) condition of junction after extended period of operation.
Parasitic Channels and Charge Spreading

Parasitic PMOS in a standard bipolar process (a) and parasitic NMOS in an N-well CMOS process (b).
Charge Spreading

Cross section of a standard bipolar structure susceptible to charge spreading: (a) before and (b) after an extended period of operation under bias.
Parasitic PMOS Channel Formation

Example of a circuit susceptible to parasitic PMOS channel formation.
Preventing PMOS Channels

Two methods for preventing parasitic PMOS channels: (a) channel stops prevent channel formation beneath leads but do not stop charge spreading and (b) field plates provide relatively complete coverage, except possibly in the gap between the plates.
Improved field plating schemes: (a) flanged field plates and (b) combination of field plates and channel stops.
Partial Field Plate

Example of partial field plating.
Elimination of Parasitic PMOS Channel

The parasitic PMOS channel beneath a poly lead (a) can be eliminated by pulling poly inside the well (b).
Prevention of NMOS Channels

Sample layout showing the use of PSD rings to prevent NMOS channels.
Parasitics
Substrate Debiasing

Cross section of a standard bipolar die showing potential substrate debiasing caused by substrate resistance $R_s$. 
Forward Voltages of Typical Collector-Substrate Junction

<table>
<thead>
<tr>
<th>Current</th>
<th>25 °C</th>
<th>85 °C</th>
<th>125 °C</th>
<th>150 °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>10nA</td>
<td>0.43V</td>
<td>0.29V</td>
<td>0.19V</td>
<td>0.13V</td>
</tr>
<tr>
<td>100nA</td>
<td>0.49V</td>
<td>0.36V</td>
<td>0.27V</td>
<td>0.22V</td>
</tr>
<tr>
<td>1 μA</td>
<td>0.55V</td>
<td>0.43V</td>
<td>0.35V</td>
<td>0.30V</td>
</tr>
<tr>
<td>10 μA</td>
<td>0.61V</td>
<td>0.50V</td>
<td>0.43V</td>
<td>0.39V</td>
</tr>
<tr>
<td>100 μA</td>
<td>0.67V</td>
<td>0.57V</td>
<td>0.51V</td>
<td>0.47V</td>
</tr>
</tbody>
</table>

Forward voltages for a typical collector-substrate junction of a minimum NPN transistor in standard bipolar, as a function of temperature and current.
Simplified model of substrate debiasing in a standard bipolar process.
Minority-Carrier Injection

Example of minority-carrier injection into the substrate of a standard bipolar process. Lateral NPN transistor $Q_P$ models the transit of minority-carries across the isolation.
Parasitic BJTs of CMOS

(a) Cross section of a CMOS die showing diffusions that form the two parasitic bipolar transistors $Q_P$ and $Q_N$; (b) equivalent schematic showing these transistors along with well resistance $R_1$ and substrate resistance $R_2$. 

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Electron-Collecting Minority-Carrier Guard Ring

Sample electron-collecting minority-carrier guard ring \((T_3)\) implemented in a standard bipolar process.
Electron-Collecting Guard Ring

Cross sections of two representative electron-collecting guard rings: (a) standard bipolar and (b) CMOS.
Improved Minority-Carrier Guard Ring

Cross sections of an improved minority-carrier guard ring for collecting electrons injected into the substrate.
Collecting Holes into a Tank

Cross sections of a minority-carrier guard ring for collecting holes injected into a tank.
Matching capacitors using identical area-to-periphery ratios.

Effects of epitaxy on surface discontinuities (a) pattern shift, (b) pattern distortion, and (c) pattern washout.
Layout showing an intersection of the NBL shadow with the leftmost base resistor.
Variations in etch rate in an array of supposedly matched resistors. The exposed outer edges of the resistors experience overetching relative to the protected inner edges.

Examples of (a) unconnected dummy resistors and (b) connected dummy resistors.
Matched capacitor array employing grounded dummies. The metal-2 electrostatic shield covering this array has been omitted for clarity.
Matched array of diffused base resistors including grounded dummies.
Examples of additional opportunities for reducing diffusion interactions (a) poor serpentine resistor layout and (b) improved layout; (c) poor placement of deep-N+ sinker and (d) improved placement.
Isobaric contour plot of the stress distribution across the surface of a typical epoxy-mounted plastic-packaged (100) silicon die, together with two graphs showing the stress along section lines A-A and B-B.
Isobaric contour plot showing regions of highest and lowest stress gradient.
Locations for placing common centroid arrays on (100) and (111) dice, in the latter case assuming an axis of distribution around the <211> axis.
Typical thermal impedances for several common types of packages.

<table>
<thead>
<tr>
<th>Type of package</th>
<th>$\Theta_{ja}$ (°C/W)</th>
<th>$\Theta_{jc}$ (°C/W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>16-pin plastic dual in-line package (DIP)</td>
<td>110</td>
<td></td>
</tr>
<tr>
<td>16-pin plastic surface-mount package (SOIC)</td>
<td>131</td>
<td></td>
</tr>
<tr>
<td>3-lead plastic TO-220 power package</td>
<td>4.2</td>
<td></td>
</tr>
<tr>
<td>3-lead metal TO-3 can power package</td>
<td>2.7</td>
<td></td>
</tr>
</tbody>
</table>

Isothermal contour plot of a die having only one major heat source. The axis of symmetry of the thermal distribution is marked by a dotted line.
Various arrangements of one, two, and four power devices for optimal thermal matching. The power devices are shown as dark gray rectangles, and the axes of symmetry created by their placement are shown as dotted lines.
(a) Improper connection of resistor segments causes their thermoelectric potentials to add, while (b) proper connection of the segments cancels the thermoelectrics.
An HSR resistor with widely separated contacts (a) is prone to thermoelectric-induced offsets. Placing the contacts close together (b) minimizes thermoelectrics, but may increase variation due to misalignment. Placing the contacts close together and oriented in opposite directions (c) fixes both problems.
Two HSR resistors connected in order to cancel both thermoelectrics and tank modulation effects.
Portion of an interdigitated HSR array implemented in a single-level metal process showing the placement of a jumper between segments.
The concept of an electrostatic shield: (a) cross section and (b) equivalent circuit.
Example of electrostatic shielding applied to a matched poly resistor array.
HSR resistor array, field-plated to minimize charge spreading. With the exception of its metallization pattern, this array matches the one in page 52.
HSR resistor array, field-plated to minimize dielectric polarization as well as to charge spreading and thermoelectrics (compare with page 56).
Cross section of a poly-poly capacitor incorporating an electrostatic shield plate. Note the overlap of the electrostatic plate over the upper electrode.
Chapter 4 Layout of MOS Transistor

- Basic MOS Transistor
- HSPICE Description of MOSFET
- MOS Devices Layout Styles
- Common Centroid Layout
Basic NMOS Layout & Side View

Circuit Symbol
HSPICE Parameter HDIF

LD : Lateral Diffusion.
LDIF : Lightly Doped Drain or Source.
HDIF : LDIF edge to contact center.
ACM = 2 (Hspice Default)

Calculation of $AD(AS)$, $PD(PS)$, $NRD(NRS)$

$AD_{eff} = 2 \cdot HDIF \cdot Weff$

$AS_{eff} = 2 \cdot HDIF \cdot Weff$

$PD_{eff} = 2 \cdot (2 \cdot HDIF + Weff)$

$PS_{eff} = 2 \cdot (2 \cdot HDIF + Weff)$

$$R_{Deff} = \frac{RDC}{M} + \frac{HDIF \cdot RSH + (LD + LDIF) \cdot RD}{Weff}$$

$$R_{S eff} = \frac{RSC}{M} + \frac{HDIF \cdot RSH + (LD + LDIF) \cdot RS}{Weff}$$
ACM = 3 (Human Work)

GEO=0: Drain and Source are not shared (default).
GEO=1: Drain is shared with another device.
GEO=2: Source is shared with another device.
GEO=3: Drain and Source are shared with another device.
Example of GEO Description (3-input NAND)
Contact Resistance

(a) Layout

(b) Equivalent circuit

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MOS Devices Layout Styles

Current flow direction

Equivalent squares (n=5 as shown)

(W/L) = (W_1 + W_2 + 0.6L)/L

(W/L) = (W_1 + W_2 + 1.1L)/L

[A] Layout

[B] Equivalent circuit

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Device Scaled Down
Minimum Width vs. Minimum Area Device

TSMC 0.25um
• The minimum channel width is 0.3um but its device is not smallest.
A Wide Digital Transistor Layout

Active Area
Poly
Metal
Contact

S
G
D

D
G
S
Stacked Wide Transistor

- **S**: Source
- **G**: Gate
- **D**: Drain

- **Active Area**
- **Poly**
- **Metal**
- **Contact**
Stacked Layout

- reduction of silicon area
- reduction of parasitic capacitance
- unmatched undercut will determine slight different lengths
- metal lines run outside the active area to ensure best contact of source and drain
- inner gates see the same boundary condition
- low sensitive to implant tilt

Implant Tilt
Stacked Layout

- minimize the source or drain contact area by stacking transistors
- respect the symmetries that exist in the electrical network as well as in the layout (to limit offset)
- use low resistive paths (metal, not poly) when a current needs to be carried (to avoid parasitic voltage drop)
- shield critical nodes (to avoid undesired node injection)
- it’s possible to enlarge or to diminish the width of a transistor to stack it with other transistors of the cell in a full stacked arrangement
- benefits of reducing the parasitics
- easier to achieve matching and to respect the electrical symmetries
Comparisons of MOS Devices Layout Styles

(a) \( w \)

(b) \( w/2 \)

(c) \( w/4 \)

(d) \( w \)

(e) \( w/2 \)
Waffle Layout
Bent-Gate
JOGM

\[ L_{\text{chain}} \]

\[ S_{\text{mid}} \]

\[ D_{\text{min}} \]

\[ L_{T-JOGM} \]

\[ D_{\text{con}} \]
Matched Transistor Paris in Increasing Order of Matching
Poor Layout with Different Orientation
Stacked Layout
Effect of Gradient in a Differential Pair
Stacked Layout One-Dimensional Cross-Coupling

\[ M_{1a} \quad M_{2a} \quad M_{3a} \quad M_{4a} \]

- \( C_{ox} \)
- \( C_{ox} + \Delta C_{ox} \)
- \( C_{ox} + 2 \Delta C_{ox} \)
- \( C_{ox} + 3 \Delta C_{ox} \)

(a)

\[ M_{1b} \quad M_{2b} \quad M_{3b} \quad M_{4b} \]

- \( C_{ox} \)
- \( C_{ox} + \Delta C_{ox} \)
- \( C_{ox} + 2 \Delta C_{ox} \)
- \( C_{ox} + 3 \Delta C_{ox} \)

(b)
MOS Matching Mirror
Layout of Interdigitized Stacked Differential Pair
Layout of Differential Pair

(a)

(b)

(c)

(d)
Differential Pair Layout with Non-Equivalent Parasitic

[Diagram showing differential pair layout with non-equivalent parasitics, including active area, poly, metal, and contact elements.]
Common-Centroid Layout Differential Pair
Layout of Differential Pair
Common-Centriod Layout of Differential Pair
Layout of Differential Pair

Layout of differential pair showing (a) normal, (b) interdigitized, and (c) common centroid.
Interdigitized Layout
Interdigitized Layout
Interdigitized Layout
Floating Source
Guard Ring

- p+ diffusion in p-substrate (p-well), tied to Vss
- n+ diffusion in n-well, tied to VDD
- collect injected minority carriers
Parasitic BJT

Lateral bipolar pnp: emitter p+, base n-well, collector p-substrate
Bipolar Model

<table>
<thead>
<tr>
<th>Model</th>
<th>PNP 10</th>
<th>PNP 5</th>
<th>PNP 2</th>
</tr>
</thead>
<tbody>
<tr>
<td>Emitter size</td>
<td>10*10</td>
<td>5*5</td>
<td>2*2</td>
</tr>
<tr>
<td>Base size</td>
<td>16*16</td>
<td>11*11</td>
<td>8*8</td>
</tr>
</tbody>
</table>
PNP x 9
Capacitance Estimation

The total load capacitance on the output of an MOS gate:
1. sum of gate capacitance
   (of other inputs connected to the output of the gate),
2. diffusion capacitance
   (of the drain/source regions connected to the output)
3. routing capacitance
   (of connections between the output and other inputs).
**MOS Device Capacitances**

$\begin{align*}
C_{gs}, \quad C_{gd} &= \text{gate to channel capacitances, which are lumped at source and drain regions of channel, respectively.} \\
C_{sb}, \quad C_{db} &= \text{source and drain diffusion capacitances to bulk (or substrate).} \\
C_{gb} &= \text{gate to bulk capacitance.}
\end{align*}$

The total gate capacitance  

$C_g = C_{gb} + C_{gs} + C_{gd}$
MOS Device Capacitances

1. off region, $V_{gs} < V_{t}$, no channel,
   $C_{gs} = C_{gd} = 0$
   $C_{gb} = C_{o} \cdot \frac{C_{dep}}{(C_{o} + C_{dep})}$

2. linear region, $V_{gs} - V_{t} > V_{ds}$
   depletion region layer depth remains relatively constant,
   $C_{gs} = C_{gd} = \frac{1}{2} \frac{\varepsilon_{sio^{2}} \varepsilon_{o}}{t_{ox}} A$

3. saturation region, $V_{gs} - V_{t} < V_{ds}$
   channel heavily inverted, drain region pinch off
   $C_{gd} = 0$
   $C_{gs} = \frac{2}{3} \frac{\varepsilon_{sio^{2}} \varepsilon_{o}}{t_{ox}} A$
Diffusion Capacitances

$C_d \propto$ total diffusion-to-substrate junction capacitance

$C_d = C_{ja} \cdot (ab) + C_{jp} \cdot (2a+2b)$

$C_{ja}$: junction capacitance per um$^2$

$C_{jp}$: peripheral capacitance per um

$a$: width of diffusion region (um)

$b$: length of diffusion region (um)
Source/Drain Area and Peripheral

[p, Na,sw] Sidewall

Bottom

[n+, Nd] Sidewall

[p, Na,sw] Bottom (bulk) doping

[VR] Perimeter

[n+, Nd] Article

[Area=A] Gate

[oxide] n+, Nd

[p, Na,sw] n+, Nd

[p, Na] Oxide

[X_j] p, Na
Diffusion Capacitances

- As the diffusion area is reduced through scaling, the relative contribution of the peripheral capacitance becomes more important.
- The thickness of the depletion layer depends on the voltage across the junction, the junction capacitance

\[ C_j = C_{j0} \left(1 - \frac{V_j}{V_b}\right)^{-m} \]

where

- \( V_j \): junction voltage (negative for reverse bias)
- \( C_{j0} \): zero bias capacitance (\( V_j = 0 \))
- \( V_b \): built-in junction potential ~ 0.6V
- \( m \): constant, depends on the distribution of impurity near the junction
  - \( m=0.3 \) (graded junction)
  - \( m=0.5 \) (abrupt junction)
Voltage Dependent Diffusion Capacitance

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C_j(V_R)

V_R

C_j0

n^+, N_d

p, N_a

Gate

oxide

n^+, N_d

Reverse Leakage current

V_R
HSPICE Description of MOSFET

Mxxx nd ng ns nb mname L=length W=width
+ AD=val AS=val PD=val PS=val
+ NRD=val NRS=val M=val GEO=val

e.g.

MP1 Drain Gate Source Bulk pmos L=0.25U W=3.60U
+ AD=1.33P AS=1.85P PD=6.56U PS=9.52U
+ NRD=0.061 NRS=0.061 M=1 GEO=0
HSPICE Description of MOSFET

Mxxx : MOSFET element name.
nd : Drain terminal node name.
ng : Gate terminal node name.
ns : Source terminal node name
nb : Bulk terminal node name
mname : MOSFET model name.
L : MOSFET channel length.
W : MOSFET channel width.
AD : Drain bottom area.
AS : Source bottom area.
PD : Peripheral of the drain junction, including the channel edge.
PS : Peripheral of the source junction, including the channel edge.
NRD : Number of squares of drain diffusion for resistance calculations.
M : Multiplier to simulate multiple MOSFETs in parallel.
GEO : Source/Drain sharing selector for MOSFET model.
## 2.5V Nominal Vt device model

<table>
<thead>
<tr>
<th>W/L</th>
<th>100/20</th>
<th>1.2/20</th>
<th>0.6/20</th>
<th>0.3/20</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(100/20)</td>
<td>(1.2/20)</td>
<td>(0.6/20)</td>
<td>(0.3/20)</td>
</tr>
<tr>
<td></td>
<td>N,pch.1</td>
<td>N,pch.2</td>
<td>N,pch.3</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>L</th>
<th>100/1.2</th>
<th>1.2/1.2</th>
<th>0.6/1.2</th>
<th>0.3/1.2</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(100/1.2)</td>
<td>(1.2/1.2)</td>
<td>(0.6/1.2)</td>
<td>(0.3/1.2)</td>
</tr>
<tr>
<td></td>
<td>N,pch.6</td>
<td>N,pch.7</td>
<td>N,pch.8</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>100/0.5</th>
<th>1.2/0.5</th>
<th>0.6/0.5</th>
<th>0.3/0.5</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(100/0.5)</td>
<td>(1.2/0.5)</td>
<td>(0.6/0.5)</td>
<td>(0.3/0.5)</td>
</tr>
<tr>
<td></td>
<td>N,pch.3</td>
<td>N,pch.6</td>
<td>N,pch.9</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>100/0.24</th>
<th>1.2/0.24</th>
<th>0.6/0.24</th>
<th>0.3/0.24</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(100/0.24)</td>
<td>(1.2/0.24)</td>
<td>(0.6/0.24)</td>
<td>(0.3/0.24)</td>
</tr>
</tbody>
</table>
Random Mismatches due to Microscopic Variations
Reduction of Length Mismatch as a Result of Increasing the Width

\[ \Delta L1 \]

\[ \Delta L2 \]
Wide MOSFET Viewed as a Parallel Combination of Narrow Devices
Large MOSFET Viewed as a Combination of Small Devices
Isothermal

differential pairs

isotherms

good

bad

power devices
Chapter 5  Layout of Bipolar Transistor

- Bipolar Transistor Operation
- Standard Bipolar Small-Signal Transistors
- Alternative Small-Signal Bipolar Transistors
- Bipolar Transistors in a CMOS Process
Topics in bipolar transistor operation

Simplified three-terminal model of an NPN transistor.

Beta versus collector current plots for small-signal NPN and lateral PNP transistors. The curve marked in gray shows the effect of emitter-base avalanche on NPN base.
Idealized curve tracer plots of $V_{CEO}$, $V_{CER}$, and $V_{CES}$ in an NPN transistor.
Forward-bias safe operating area (FBSOA) plot of a typical NPN power transistor.
Cross section of an NPN transistor fabricated on a standard bipolar process, showing the parasitic PNP transistor.
An example of a circuit that exhibits current hogging. $Q_P$ represents the parasitic PNP transistor present in the structure of vertical NPN $Q_3$.

Base-side ballasting applied to the circuit shown above.
A base-side ballasting resistor becomes ineffective when merged into the same tank as the NPN it protects.

(a) Schottky-clamped NPN transistor and (b) its conventional schematic symbol.
Cross section of a lateral PNP transistor constructed on a standard bipolar process showing parasitic substrate PNP transistors $Q_{P1}$ and $Q_{P2}$. 
Symbols for three-terminal and four-terminal transistors (E: emitter, B: base, C: collector, S: substrate).

Subcircuit models for (a) vertical NPN transistor and (b) lateral PNP transistor.
Standard Bipolar Small-Signal Transistors

- Heavily doped emitter diffusion (junction depth set emitter pilot)
- Deep-N+plug minimizes vertical collector resistance
- NBL minimizes lateral collector resistance
- Base doping and junction depth optimized for NPN transistor
- Lightly doped N-epi forms collector drift region

Key features of the standard bipolar vertical NPN transistor.

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Two styles of NPN transistors: (a) collector-emitter-base (CEB), and (b) collector-base-emitter (CBE).
Three examples of stretched NPN transistors.
(a) Layout of a compact emitter NPN transistor and (b) a cross section of the active region of this device that illustrates the effects of emitter crowding.
(a) The narrow-emitter transistor and (b) its equivalent minimum-size layout, the double-base transistor.
Cross section of a typical substrate PNP transistor fabricated in standard bipolar.
Example of (a) standard, (b) emitter-ring, and (c) verti-lat styles of substrate PNP transistor.

Higher-current substrate PNP transistor employing two wide emitter stripes and a single narrow base stripe.
Cross section of a lateral PNP transistor depicting three different measures of neutral base width discussed in the text (drawn base width, $W_{B1}$, actual base width at the surface, $W_{B2}$, and effective base width beneath the surface, $W_{B3}$.

Layout of a lateral PNP transistor showing emitter field plate.
Example of split collector transistors: (a) $\frac{1}{2} - \frac{1}{2}$ (b) $\frac{1}{4} - \frac{1}{4} - \frac{1}{4} - \frac{1}{4}$, (c) $\frac{1}{6} - \frac{1}{6} - \frac{1}{6} - \frac{1}{4} - \frac{1}{4}$. The field plates have been omitted for clarity.
Schematic diagrams for 1:1 current mirrors constructed using split collector lateral PNP transistors: (a) conventional schematic diagram and (b) simplified schematic diagram.

Square geometry lateral PNP transistors: (a) minimum-emitter and (b) ½- ½ split collector. The field plates have been omitted for clarity.
Higher-current lateral PNP transistors: (a) elongated-emitter or hotdog transistor and (b) a small arrayed-emitter transistor.
High-voltage Bipolar Transistors

NPN transistors incorporating high-voltage fillets (a) on base only and (b) on base, NBL, and isolation.
Alternative Small-Signal Bipolar Transistors

Comparison of representative cross sections of (a) a standard bipolar NPN and (b) a super-beta NPN.

Comparison of representative cross sections of (a) a standard bipolar lateral PNP and (b) a deep-P+ lateral PNP.
Analog BiCMOS Bipolar Transistors

Comparison of saturation characteristics of CDI NPN transistors with and without the addition of deep-N+ sinkers.
Layout and cross section of an extended-base NPN transistor.
Bipolar Transistors in a CMOS Process

Layout of a substrate PNP transistor compatible with an N-well CMOS process.
Advanced-technology Bipolar Transistors

Comparison between (a) a conventional diffused emitter and (b) a washed emitter.

Layout and cross section of a CDI NPN transistor with a polysilicon emitter.
Partial oxide-isolated NPN transistors: (a) conventional, and (b) walled-emitter.

Cross section of a super self-aligned transistor.
Bipolar Gummel-Poon Model

<table>
<thead>
<tr>
<th>Model</th>
<th>PNP 10</th>
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<th>PNP 2</th>
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<tr>
<td>Base size</td>
<td>16*16</td>
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</tr>
</tbody>
</table>
PNP x 9
Chapter 6  Layout of Resistor

- Resistance Estimation
- Resistivity and Sheet Resistance
- Resistor Layout
- Resistor Variability
- Resistor Parasitics
- Comparison of Available Resistors
- Adjust Resistor Values
# Resistivities

<table>
<thead>
<tr>
<th>Material</th>
<th>Resistivity $\Omega \cdot \text{cm (25 } ^\circ \text{C)}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Copper, bulk</td>
<td>$1.7 \cdot 10^{-6}$</td>
</tr>
<tr>
<td>Gold, bulk</td>
<td>$2.4 \cdot 10^{-6}$</td>
</tr>
<tr>
<td>Aluminum, thin film</td>
<td>$2.7 \cdot 10^{-6}$</td>
</tr>
<tr>
<td>Aluminum (2% silicon)</td>
<td>$3.8 \cdot 10^{-6}$</td>
</tr>
<tr>
<td>Platinum silicide</td>
<td>$3.0 \cdot 10^{-6}$</td>
</tr>
<tr>
<td>Silicon, N-type ($N_d = 10^{18} \text{ cm}^{-3}$)</td>
<td></td>
</tr>
<tr>
<td>Silicon, N-type ($N_d = 10^{15} \text{ cm}^{-3}$)</td>
<td></td>
</tr>
<tr>
<td>Silicon, intrinsic</td>
<td>$2.5 \cdot 10^5$</td>
</tr>
<tr>
<td>Silicon dioxide ($\text{SiO}_2$)</td>
<td>$\sim 10^{14}$</td>
</tr>
</tbody>
</table>
Resistance Estimation

The resistance of a uniform slab of conducting material

\[ R = \frac{\rho \ell}{A} = \frac{\rho \ell}{t \, w} = R_s \frac{\ell}{w} \]

- \( \rho \) : resistivity
- \( t \) : thickness
- \( \ell \) : conductor length
- \( w \) : conductor width
- \( R_s \) : sheet resistance
Interconnections and Contacts/Vias

- Put barrier metal (typically platinum) to reduce the contact resistance and the likelihood of breaks in the contact.
- Use chemical-mechanical polishing (CMP) to smooth the wafers flat before each metal deposition step to help with step coverage.
- Insulator between layers – SiO₂
## Contact Resistance Parameters

<table>
<thead>
<tr>
<th>Contact/via type</th>
<th>Resistance (maximum)</th>
<th>Contact resistance (1 μm CMOS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>m2/m3 via(via2)</td>
<td>5 Ω</td>
<td></td>
</tr>
<tr>
<td>m1/m2 via(via1)</td>
<td>2 Ω</td>
<td></td>
</tr>
<tr>
<td>m1/p-diffusion contact</td>
<td>20 Ω</td>
<td></td>
</tr>
<tr>
<td>m1/n-diffusion contact</td>
<td>20 Ω</td>
<td></td>
</tr>
<tr>
<td>m1/poly contact</td>
<td>20 Ω</td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Contact/via type</th>
<th>Resistance (maximum)</th>
<th>Contact resistance (0.35 μm CMOS)</th>
</tr>
</thead>
<tbody>
<tr>
<td>m2/m3 via(via2)</td>
<td>6 Ω</td>
<td></td>
</tr>
<tr>
<td>m1/m2 via(via1)</td>
<td>6 Ω</td>
<td></td>
</tr>
<tr>
<td>m1/p-diffusion contact</td>
<td>20 Ω</td>
<td></td>
</tr>
<tr>
<td>m1/n-diffusion contact</td>
<td>20 Ω</td>
<td></td>
</tr>
<tr>
<td>m1/poly contact</td>
<td>20 Ω</td>
<td></td>
</tr>
</tbody>
</table>
Silicide and Salicide

Diffusion – n⁺ or p⁺

Silicide poly gate – e.g. metallic compound of silicon
  Tantalum silicide TaSi,
  Tungsten silicide WSi,
  or Titanium silicide TiSi

Salicide (self-aligned silicide)
– both gate and source/drain regions are silicided
Resistor Types

Poly

well

diffusion

N -well

P+diffusion

P-SUB

P-SUB guard ring

P+

N -well
Resistor Types

Poly

well

diffusion
# Sheet Resistance Parameters

<table>
<thead>
<tr>
<th>Layer</th>
<th>Sheet resistance</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>n-well</td>
<td>1.15 ± 0.25</td>
<td>kΩ/square</td>
</tr>
<tr>
<td>poly</td>
<td>3.5 ± 2.0</td>
<td>Ω/square</td>
</tr>
<tr>
<td>n-diffusion</td>
<td>75 ± 20</td>
<td>Ω/square</td>
</tr>
<tr>
<td>p-diffusion</td>
<td>140 ± 40</td>
<td>Ω/square</td>
</tr>
<tr>
<td>m1/2</td>
<td>70 ± 6</td>
<td>mΩ/square</td>
</tr>
<tr>
<td>m1/2</td>
<td>30 ± 3</td>
<td>mΩ/square</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Layer</th>
<th>Sheet resistance</th>
<th>Units</th>
</tr>
</thead>
<tbody>
<tr>
<td>n-well</td>
<td>1 ± 0.4</td>
<td>kΩ/square</td>
</tr>
<tr>
<td>poly</td>
<td>10 ± 4.0</td>
<td>Ω/square</td>
</tr>
<tr>
<td>n-diffusion</td>
<td>3.5 ± 2.0</td>
<td>Ω/square</td>
</tr>
<tr>
<td>p-diffusion</td>
<td>2.5 ± 1.5</td>
<td>Ω/square</td>
</tr>
<tr>
<td>m1/2/3</td>
<td>60 ± 6</td>
<td>mΩ/square</td>
</tr>
<tr>
<td>metal4</td>
<td>30 ± 3</td>
<td>mΩ/square</td>
</tr>
</tbody>
</table>
Resistor Equivalent Circuit Model

1) Circuit Models for AC Effect of Diffused and Ion- Implanted Resistors

Cross section of Diffused and Ion-implanted Resistor
Cross section of a base pinch resistor showing the intrusion of the depletion regions into the neutral base. Notice that the high-voltage end of the resistor narrows slightly.
The following functions have been implemented the model:

1. Resistor values are function of temperature:

   \[ R(t) = R_0 \left[ 1 + TC1 \cdot dT + TC2 \cdot (dT)^2 \right] \]

   Where: \( dT = T - T_{nominal} \) (25°C)

   Valid range: \( 25°C \sim 125°C \)

2. Resistor values are function of temperature:

   \[ R(V) = R_0 \left[ 1 + VC1 \cdot dV + VC2 \cdot (dV)^2 \right] \]

   Valid range: \( 0 \sim 2V \)

**Resistor size (drawn):** \( L, W \)

- DA: area = \((W - \text{delta} W) \times L/5\)
- pj = \((W - \text{delta} W) + 2 \times L/5\)
- DB: area = \((W - \text{delta} W) \times L/5\)
- pj = \(2L/5\)
- R: value = \(rsh \times L/(4(W - \text{wdelta} W))\)
2) Circuit Models for N+ / P+ Poly w/o Silicide Resistor

Resistor Size (drawn) : L,W
R=2*Rcon+ 2*Rend+Rp
Rcon=Rc/nc (note)
Rend=Rint / (W-DeltaW)
Rp=Rsh*(L-DeltaL) / (W-DeltaW)

Note : nc is Number of Contact, and its default value is 2
Resistor consisting a rectangular Slab contacted by perfectly conducting terminations

\[ R = R_s \frac{L_d}{(W_d + W_b)} \]

Wb : width bias, difference between drawn width and effective width
Layout of serpentine resistors with rectangular turns and circular turns

\[ R = R_s[(2A+B)/W+1.12] \]

\[ R = R_s(2C/W+2.96) \]
Dummy
NW resistance

NW within OD

Rs_NW under different NW dimension

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NW under STI

Rs_NW under different STI thickness

Rs_NW v.s. NW width

T

STI thickness

Width of NW (um)
Isothermal

(a) Power Device
(b) Power Device
Cross section of a polysilicon resistor.

Subcircuit models for polysilicon resistors that approximate distributed substrate capacitance using π-sections (a) single π-section and (b) dual π-section.
Resistor layout

no matching issue
not care absolute value
small size

no matching issue
care absolute value
Interdigitized Layout of Resistor
care matching
not care absolute value ↓

finger layout

↑
care matching and absolute value ↓

R1 R2
Square

Poly 44 ohm/square

$\frac{100}{44} = 2.272 \text{ square}$

Length = $2.272 \times 4 = 9.1 \mu m$

Unit cell layout

ex: $500 \text{ ohm} = 100 \text{ ohm} \times 5$
Consideration of dummy

The resistor cells are layouted into square as possible add the dummy cells at four sides.
Crosses resistor
Well

Substrate bias
- Place shield under resistor that is connected to clean power supply
- N-well region to keep substrate noise from being injected into conductive layer
- Noise is due to capacitively coupling between substrate and a large resistor structure
- The parasitic capacitor between resistor and the shield should be modeled during simulation

For low-noise design, a metal shield over the top maybe necessary
-- With resistor of high values (KΩ or MΩ), use n-well (or p-well)
Common Centroid
Correction factors $\Delta R$ for dogbone resistors

<table>
<thead>
<tr>
<th>$W_o$</th>
<th>$W_c$</th>
<th>$\Delta R$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$W_d$</td>
<td>$W_d$</td>
<td>-0.7</td>
</tr>
<tr>
<td>$1/2W_d$</td>
<td>$W_d$</td>
<td>-0.3</td>
</tr>
</tbody>
</table>
Sample dogbone and serpentine resistors, showing the poor packing density caused by the presence of enlarged heads.
Typical linear temperature coefficients of resistivity for selected materials at 25°C

<table>
<thead>
<tr>
<th>Material</th>
<th>TCR , ppm/ °C</th>
</tr>
</thead>
<tbody>
<tr>
<td>Aluminum, bulk</td>
<td>+3800</td>
</tr>
<tr>
<td>Copper, bulk</td>
<td>+4000</td>
</tr>
<tr>
<td>Gold, bulk</td>
<td>+3700</td>
</tr>
<tr>
<td>$160 \Omega$ Base diffusion</td>
<td>+1500</td>
</tr>
<tr>
<td>$7 \Omega$ Emitter diffusion</td>
<td>+600</td>
</tr>
<tr>
<td>$5k \Omega$ Base pinch diffusion</td>
<td>+2500</td>
</tr>
<tr>
<td>$5k \Omega$ HSR implant (P-type)</td>
<td>+3000</td>
</tr>
<tr>
<td>$500 \Omega$ Polysilicon (4kÅ N-type)</td>
<td>-1000</td>
</tr>
<tr>
<td>$25 \Omega$ Polysilicon (4kÅ N-type)</td>
<td>+1000</td>
</tr>
<tr>
<td>$10k \Omega$ N-well</td>
<td>+6000</td>
</tr>
</tbody>
</table>
## Typical contact resistances for various contact systems.

<table>
<thead>
<tr>
<th>Contact System</th>
<th>Contact Resistivity, $\Omega \cdot \mu$ m²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al-Cu-Si to 160 $\Omega$ / $\square$ Base</td>
<td>750</td>
</tr>
<tr>
<td>Al-Cu-Si to 5 $\Omega$ / $\square$ Emitter</td>
<td>40</td>
</tr>
<tr>
<td>Al-Cu / Ti-W / PtSi to 160 $\Omega$ / $\square$ Base</td>
<td>1250</td>
</tr>
<tr>
<td>Al-Cu / Al-Cu (Via)</td>
<td>5</td>
</tr>
<tr>
<td>Al-Cu / Ti-W / Al-Cu (Via)</td>
<td>5</td>
</tr>
</tbody>
</table>
Cross section of a typical diffused resistor.

Subcircuit models for diffused resistors (a) neglecting tank resistance and (b) including tank resistance.
Several methods of biasing the tank connections of diffused resistors.
Layout and cross section of an alternate style of emitter resistor that eliminates the enclosing base diffusion to save space.
Layout of an HSR (High-sheet-resistance) resistor, showing relevant dimensions.

\[ R = R_s \left[ \frac{(L_d-L_b)}{(W_d-W_b)} + 2R_h \right] \]

Example of an HSR resistor with an extended head
Layout of an epi pinch resistor (epi-FET).

Two styles of Kelvin-connected metal sense resistors (a) single-level-metal layout and (b) double-level-metal layout.
High-sheet poly resistor with implanted heads.

\[
\begin{align*}
R &= R_s \left( \frac{L_d}{W_d + W_b} \right) \\
&\quad + 2R_h \left[ \frac{L_h}{W_d + W_b} \right]
\end{align*}
\]

(a) N-well resistor and (b) N-well resistor with PSD pinch plate (field plates not show.)
Layout of a thin-film resistor.

Two styles of sliding contacts (a) without heads and (b) with heads.
Layout of a resistor with a sliding head.

Resistor adjustment by means of a trombone slide.
Layouts of (a) a typical metal fuse and (b) a polysilicon fuse.
Two different binary-weighted resistor trim schemes using fuses (a) series-connected and (b) parallel-connected. Both cases assume that the ground pad is used to program the fuses.
Differential trim scheme applied to the LSB fuse, $F_2$, of a series-connected binary-weighted trim network.
Zener zap constructed using base and emitter diffusions from a standard bipolar process (a) layout of unprogrammed Zener and (b) cross section of programmed Zener.
Four different schemes for laser-trimming thin-film resistors (a) notched bar, (b) tophat, (c) looped layout, and (d) ladder layout. The heavy black lines show the path of the laser beam through the resistor.
The Silicide Block of Poly Resistor

Silicide Block

Silicided Poly

FOX

POLY

P-substrate

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N-Well Resistor

N-Well

P-substrate
\[ R = 82.94 \times 20 \Omega / \square = 1.659k \Omega \]
Resistor ladder used in an A/D converter

\[ V_1 \]

\[ R_1 \]

\[ V_{\text{REF}127} \]

\[ R_{127} \]

\[ V_{\text{REF}128} \]

\[ R_{128} \]

\[ V_2 \]
Resistor Ladder Made of Metal
Chapter 7 Layout of Capacitor

- Routing Capacitance
- Capacitance
- Capacitor Variability
- Capacitor Parasitics
- Comparison of Available Capacitors
- Layout of Capacitors
- Varactors
Routing Capacitance

two components
- parallel-plate capacitance
- fringing field
Capacitive Coupling Components

(a) Fringing-field capacitance
(b) Lateral (inter-wire) capacitance
Parallel-plate capacitance

Overlap and fringing-field capacitance
Inter-wire
Parallel-plate capacitance

Graph showing capacitance vs. design rule (μm)
- CTOTAL
- Cx
- CGROUND
- CPP

1 μm FIELD OXIDE
1 μm METAL
1 μm Sin CAP LAYER
Each layer is perpendicular to its bottom and top layer to reduced overlapped capacitance and increase complexity of wire routing.
Variation of Fringing-Field Factor

![Diagram of current flow and fringing fields]

![Graph showing variation of FF with W/l and t/h]

FF = \frac{C}{C_{PP}}

(Parallel-plate capacitance)
Multiple Conductor Capacitance

three conductor layer
- top ground plane
- conductor of interest
- bottom ground layer

\[ C_2 = C_{21} + C_{23} + C_{22} \]

where

- \( C_2 \): middle layer 2 to ground
- \( C_{21} \): middle layer 2 to layer 1
- \( C_{23} \): middle layer 2 to layer 3
- \( C_{22} \): capacitance between other parallel conductor on layer 2

\( C_{21} \) and \( C_{23} \) given by formula for crossover capacitance

\( C_{22} \) affected by the presence or absence of layer-1 and layer-3

\( C_{22} \) total capacitance of layer-2 to layer-2 capacitance
Fringe Component of Capacitance

Substrate

Fringe Lines
Conductor Capacitance vs. Spacing

- Calculated directly from parameters, complicated for large circuits
- Weight factor model, depends on thickness and separation
- Missing neighbor model, look-up table, detect the presence or absence of adjacent conductor segments,
- Drawn dimension, actual dimension after process, dielectric thickness variation
  ★ Maximum width and minimum thickness for delay and power calculation
  ★ Minimum width and maximum thickness dielectric for race calculation
  ★ Minimum width of conductors for RC delay calculation
Parasitic Capacitance Values in 0.8µm Process

<table>
<thead>
<tr>
<th></th>
<th></th>
<th>Area</th>
<th>Perimeter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly over field oxide</td>
<td>$C_{pf}$</td>
<td>0.066 fF/μm²</td>
<td>0.046 fF/μm</td>
</tr>
<tr>
<td>Metal - 1 over field oxide</td>
<td>$C_{m1f}$</td>
<td>0.030 fF/μm²</td>
<td>0.044 fF/μm</td>
</tr>
<tr>
<td>Metal - 2 over field oxide</td>
<td>$C_{m2f}$</td>
<td>0.016 fF/μm²</td>
<td>0.042 fF/μm</td>
</tr>
<tr>
<td>Metal - 1 over poly</td>
<td>$C_{m1p}$</td>
<td>0.053 fF/μm²</td>
<td>0.051 fF/μm</td>
</tr>
<tr>
<td>Metal - 2 over poly</td>
<td>$C_{m2p}$</td>
<td>0.021 fF/μm²</td>
<td>0.045 fF/μm</td>
</tr>
<tr>
<td>Metal - 2 over Metal - 1</td>
<td>$C_{m2m1}$</td>
<td>0.035 fF/μm²</td>
<td>0.051 fF/μm</td>
</tr>
</tbody>
</table>
### Process Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Field oxide thickness</td>
<td>0.52 μm</td>
</tr>
<tr>
<td>Gate oxide thickness</td>
<td>16.0 μm</td>
</tr>
<tr>
<td>Polysilicon thickness</td>
<td>0.35 μm</td>
</tr>
<tr>
<td>Poly - metal oxide thickness</td>
<td>0.65 μm</td>
</tr>
<tr>
<td>Metal - 1 thickness</td>
<td>0.60 μm</td>
</tr>
<tr>
<td>Via oxide thickness</td>
<td>1.00 μm</td>
</tr>
<tr>
<td>Metal - 2 thickness</td>
<td>1.00 μm</td>
</tr>
<tr>
<td>n+ junction depth</td>
<td>0.40 μm</td>
</tr>
<tr>
<td>p+ junction depth</td>
<td>0.40 μm</td>
</tr>
<tr>
<td>n - well junction depth</td>
<td>3.50 μm</td>
</tr>
</tbody>
</table>

### Capacitance Calculations

<table>
<thead>
<tr>
<th>Layer Type</th>
<th>C_{pf}</th>
<th>Area</th>
<th>Perimeter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Poly over field oxide</td>
<td>C_{pf}</td>
<td>0.066 fF / μm²</td>
<td>0.046 fF / μm</td>
</tr>
<tr>
<td>Metal - 1 over field oxide</td>
<td>C_{m1f}</td>
<td>0.030 fF / μm²</td>
<td>0.044 fF / μm</td>
</tr>
<tr>
<td>Metal - 2 over field oxide</td>
<td>C_{m2f}</td>
<td>0.016 fF / μm²</td>
<td>0.042 fF / μm</td>
</tr>
<tr>
<td>Metal - 1 over poly</td>
<td>C_{m1p}</td>
<td>0.053 fF / μm²</td>
<td>0.051 fF / μm</td>
</tr>
<tr>
<td>Metal - 2 over poly</td>
<td>C_{m2p}</td>
<td>0.021 fF / μm²</td>
<td>0.045 fF / μm</td>
</tr>
<tr>
<td>Metal - 2 over Metal - 1</td>
<td>C_{m2m1}</td>
<td>0.035 fF / μm²</td>
<td>0.051 fF / μm</td>
</tr>
</tbody>
</table>
Cross Talk

- Troublesome problem in high-density layout
- Incorrect or false transition may occur.

line-to-line parasitic capacitance $C_m$
mutual inductance $L_m$
Cross Talk

Conductor 1

Conductor 2

\[ Q_1 = C_{11}V_1 + C_{12}(V_1 - V_2) \]

\[ Q_2 = C_{21}(V_2 - V_1) + C_{22}V_2 \]

\[ \Phi_1 = L_{11}I_1 + L_{12}I_2 \]

\[ \Phi_2 = L_{21}I_1 + L_{22}I_2 \]

\[ I = \frac{dQ}{dt} \quad C_m = C_{12} = C_{21} \]

\[ V_1 = L_{11}I_1 + L_{12}I_2 \]

\[ V_2 = L_{m}I_1 + L_{22}I_2 \]

\[ I_1 = C_{11} \frac{dV_1}{dt} + C_m \frac{d(V_1-V_2)}{dt} \]

\[ I_2 = C_m \frac{d(V_2-V_1)}{dt} + C_{22} \frac{dV_2}{dt} \]

\[ V = \frac{d\Phi}{dt} \quad L_m = L_{12} = L_{21} \]
Relative permittivities and dielectric strengths of selected materials

<table>
<thead>
<tr>
<th>Material</th>
<th>Relative Permittivity (Vacuum=1)</th>
<th>Dielectric Strength (MV/cm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon</td>
<td>11.8</td>
<td>30</td>
</tr>
<tr>
<td>Silicon dioxide (SiO₂)</td>
<td>Dry oxide</td>
<td>3.9</td>
</tr>
<tr>
<td></td>
<td>Plasma</td>
<td>4.9</td>
</tr>
<tr>
<td></td>
<td>TEOS</td>
<td>4.0</td>
</tr>
<tr>
<td>Silicon nitride (Si₃N₄)</td>
<td>LPVCD</td>
<td>6~7</td>
</tr>
<tr>
<td></td>
<td>Plasma</td>
<td>6~9</td>
</tr>
</tbody>
</table>
Hypothetical example of a thin – film capacitor. The crosshatched region where the two plates intersect forms the effective area of the capacitor plates, or in this case 300um².
Construction of a simple parallel – plate capacitor
Capacitor Types

MOS

Double poly

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Capacitor Types

Sandwich

Field oxide
N well
P SUB

Poly & M2 & M4
M1 & M3

M3
M4

M2

Poly

M1

M3

M4

M2

Poly
Capacitor Structure Using Various Conductive Layers

(a) C=C1
Metal4
C1
Cp
Substrate

(b) C=C1+C2
Metal4
C1
Metal4
C2
Cp
Substrate

(c) C=C1+C2+C3
Metal4
C1
Metal3
C2
Metal2
C3
Cp
Substrate

(d) C=C1+C2+C3+C4
Metal4
C1
Metal3
C2
Metal3
C3
C4
Cp
Substrate
Subcircuit models for poly-poly capacitors: (a) a simple model without series resistance, and (b) a model incorporating series resistance using single $\pi$-sections.
Subcircuit models for (a) a junction capacitor where C/E denotes the collector/emitter electrode and B denotes the base electrode; and (b) an MOS or gate oxide capacitor where G denotes the deposited gate electrode and D/S/B denotes the drain/source backgate electrode.
CTM

Capacitor dummy 1

Capacitor dummy 2

Top plate metal

CTM

Bottom plate metal

Mn+1

Where N can be 1, 2 and 3
Metal-Insulator-Metal (MIM) Capacitor
Capacitor Types

MMC

A

M5
MMC

M4

N well

P SUB

N+ N+

A'

M4 M5 CTM

Dummy layer

M5

B

A

M4

M5

CTM

M3 VIA3 VIA4

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Non-Integer Multiple of Unity Capacitor

(a)

(b)
(a) Common centroid
(b) Dummy poly2 strips
(c) Contact on top of thick oxide
(d) Matched poly2 terminals
(f) Protective well
(g) Well multiple biased
Unit Capacitor
Common-Centroid Layout of Capacitor
Capacitor Array

![Capacitor Array Diagram](image)
Capacitors Array in ADC/DAC

Short line to avoid coupling shielding of substrate noise

\[ V_{\text{in}} \rightarrow \text{OP} \rightarrow V_{\text{out}} \]

1C 2C 4C 8C 16C 64C
Illustration of the fringing field surrounding a parallel-plate capacitor embedded in a dielectric of constant permittivity.

Three-dimensional view of a diffused junction, showing the sidewalls and filleted corners produced by outdiffusion beyond the drawn dimensions of the oxide window.
Two different styles of diffusion capacitor: (a) plate and (b) comb. The tank, NBL, contact, and metal layers are omitted for clarity.

Typical schematic symbols for capacitors.
General behavior of base-emitter junction capacitance under bias. The minimum capacitance just prior to avalanche equals about 40 to 50% of the zero-bias value $C_{j0}$. 
General behavior of a MOS transistor employed as a capacitor. Different curves are obtained depending on the connection of the source and the drain.
A junction capacitor with base plates extending into isolation.
Layout and cross section of an MOS capacitor constructed in a standard bipolar process using a capacitor oxide mask.
Layout and cross section of a deep-N+ MOS capacitor constructed in an analog BiCMOS process.
Layout and cross section of a poly-poly ONO capacitor. The entire capacitor has been enclosed in NSD because the gate poly is also N-type and the additional dopant only further reduces its sheet resistance.
**Varactor**

![Varactor Diagram](image)

---

Hong-Yi Huang 黄弘一
Varactor
Varactor
Varactor
Varactor

\[ C_{ox} \]

\[ C_{mos} \]

Accumulation

Depletion

Weak inversion

Strong inversion

Moderate inversion

\[ V_{BG} \]
Varactor

\[ C_{mos} \text{ (pF)} \]

\[ V_{sg} \text{ (V)} \]

-2 -1 0 1 2

B=D=S

I-MOS
Varactor
Varactor
Varactor
Varactor
Varactor

![Graph showing carrier frequency (GHz) vs. Vctrl (V) for A-MOS, I-MOS, and DIODE.

- A-MOS line with green crosses.
- I-MOS line with red circles.
- DIODE line with blue triangles.

The x-axis represents Vctrl (V) ranging from 0 to 2.5, and the y-axis represents carrier frequency (GHz) ranging from 1.7 to 1.9.]
### Varactor

<table>
<thead>
<tr>
<th>Varactor</th>
<th>$f_L-f_H$ (GHz)</th>
<th>$f_c$ (GHz)</th>
<th>Tuning range</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diode</td>
<td>1.73-1.93</td>
<td>1.83</td>
<td>10.9%</td>
</tr>
<tr>
<td>I-MOS</td>
<td>1.71-1.91</td>
<td>1.81</td>
<td>11.0%</td>
</tr>
<tr>
<td>A-MOS</td>
<td>1.70-1.89</td>
<td>1.80</td>
<td>10.6%</td>
</tr>
</tbody>
</table>
Chapter 8  Layout of Inductor

- Inductors Layout
- Inductors Models
- Layout Styles of Inductors
- RF Spice Models
Quality of Inductor

(i) 電感值，
(ii) 品質因素 (Q)，
(iii) 共振頻率 (f_{SR})，
(iv) 晶片空間。

\[ Q = 2\pi \frac{\text{energy stored}}{\text{energy loss per cycle}} = \omega \frac{\text{energy stored}}{\text{average power loss}} \]
串聯電阻的電感\(Q\)值

\[
Q = 2\pi \frac{\text{peak magnetic energy stored}}{\text{energy loss per cycle}}
\]

\[
= 2\pi \frac{\frac{1}{2} L_s |I_s|^2}{\frac{1}{2} R_s |I_s|^2 T}
\]

\[
= \frac{\omega L_s}{R_s}
\]
並聯電阻的電感Q值

\[ Q = 2\pi \frac{\text{peak magnetic energy stored}}{\text{energy loss per cycle}} \]

\[ = 2\pi \frac{|V_p|^2}{2\omega^2 L_p} \]

\[ = 2\pi \frac{|V_p|^2}{2R_p} T \]

\[ = \frac{R_p}{\omega L_p} \]
在一般而言，品質因素的定義並不清楚的指出是能量的儲存或是消耗。

\[
Q_{\text{inductor}} = 2\pi \frac{\text{net magnetic energy stored}}{\text{energy loss per cycle}} = 2\pi \frac{\text{peak magnetic energy} - \text{peak electric energy}}{\text{energy loss per cycle}}
\]

\[
Q_{\text{tank}} = 2\pi \frac{\text{average magnetic energy} + \text{average electric energy}}{\text{energy loss per cycle}} = 2\pi \frac{\text{peak magnetic energy}}{\text{energy loss per cycle}} \bigg| \omega = \omega_0
\]

\[
= 2\pi \frac{\text{peak electric energy}}{\text{energy loss per cycle}} \bigg| \omega = \omega_0
\]
$Q_{inductor} = 2\pi \frac{\text{peak magnetic energy} - \text{peak electric energy}}{\text{energy loss per cycle}}$

$$= 2\pi \frac{\frac{|V_p|^2}{2\omega^2 L_p} - \frac{1}{2} C_p |V_p|^2}{\frac{|V_p|^2}{2R_p} T} = \frac{1}{\frac{1}{\omega L_p} - \omega C_p}$$

$$= \frac{R_p}{\omega L_p} \left[ 1 - \left( \frac{\omega}{\omega_0} \right)^2 \right]$$
\[ Q_{tank} = 2\pi \frac{\text{peak magnetic energy}}{\text{energy loss per cycle}} \bigg| \omega = \omega_0 \]

\[ = 2\pi \frac{\frac{1}{2} |V_p|^2}{\frac{1}{2} |V_p|^2} \bigg| \omega = \frac{1}{\sqrt{L_p/C_p}} \frac{R_p}{\sqrt{L_p/C_p}} \]

\[ Q_{tank} = 2\pi \frac{f}{BW_{-3db}} \bigg| f = f_0 \]

\[ = 2\pi \frac{f}{\frac{1}{2\pi R_p C_p}} \bigg| f = \frac{1}{2\pi \sqrt{L_p/C_p}} \frac{R_p}{\sqrt{L_p/C_p}} \]
實際電感的品質因素

\[
Z_{in} = \frac{1}{Y_{in}}
\]

\[
Q_{inductor} = \frac{\text{Im}\{Z_{in}\}}{\text{Re}\{Z_{in}\}} = -\frac{\text{Im}\{Y_{in}\}}{\text{Re}\{Y_{in}\}}
\]
Passive Inductor

\[ Q = 2\pi \times \frac{\text{energy stored}}{\text{average power dissipate}} = \frac{WL}{R} \]
**Inductor Layout Design Rule**

This layer is only designed for thicker top metal in the inductor circuits.

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min. width of a M5T region</td>
<td>1.5um</td>
</tr>
<tr>
<td>Min. space between two M5T region</td>
<td>1.5um</td>
</tr>
<tr>
<td>Min. area of a M5T area</td>
<td>2.25um</td>
</tr>
<tr>
<td>Min. extension of a M5T region beyond a Via4 region</td>
<td>0.3um</td>
</tr>
<tr>
<td>Min. extension of a M5T region beyond a Via4 region at the end of M5T</td>
<td>0.45um</td>
</tr>
<tr>
<td>Min. density of a M5T area ([A\text{M5T}]/A\text{chip})</td>
<td>30%</td>
</tr>
</tbody>
</table>
Inductor Layout Rule
Inductor Model

- \( L_s \): inductance
- \( R_s \): metal series resistance
- \( C_s \): overlap capacitance between the spiral and the center tap underpass
- \( C_{ox} \): oxide capacitance between the spiral and substrate
- \( R_{sub} \): silicon substrate resistance
- \( C_{sub} \): silicon substrate capacitance
## Parameter of inductor

<table>
<thead>
<tr>
<th>N</th>
<th>$R_{sub1}$ (Ohm)</th>
<th>$C_{sub1}$ (fF)</th>
<th>$R_{sub2}$ (Ohm)</th>
<th>$C_{sub2}$ (fF)</th>
<th>$Cox1$ (fF)</th>
<th>$Cox2$ (fF)</th>
<th>$Ls$ (nh)</th>
<th>$Cs$ (fF)</th>
<th>$Rs$ (Ohm)</th>
<th>$Q@1GHz$</th>
<th>$Q@2GHz$</th>
<th>Valid Freq</th>
</tr>
</thead>
<tbody>
<tr>
<td>6.5</td>
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<tr>
<td>5.5</td>
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<td>4.5</td>
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<tr>
<td>3.5</td>
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<td>2.5</td>
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</tr>
</tbody>
</table>
Layout Rule

(1) Solid inductor
(2) With Guard Ring
(3) Part of Guard Ring
Reduce Substrate Resistance

When inductor with Guard Ring, then Q is increasing

![Graph showing the relationship between frequency and parasitic inductance for different substrate resistances. The graph includes curves for Rsub = 369.5Ω and Rsub = 300Ω.]
With the same inductances value, the series resistance is:

the square inductor > the octagon inductor > the circle inductor

So the Q is circle > octagon > square inductor
Stack Inductor

\[ c_{eq} = \frac{1}{12} (4c_1 + c_2) \quad \text{For two layers} \]

\[ c_{eq} = \frac{1}{3n^2} \left( 4\sum_{i=1}^{n-1} c_i + c_n \right) \quad \text{For n-layers} \]

1. Stack inductor is the considerable increase of the overall inductance
2. Stack inductor inductance is higher than planar spiral inductor (300%) the Q is reduced by more than 50%
3. For the same inductance value, there is an area reduction
4. With the increasing distance between two layers, increasing of the self-resonance frequency and decreasing of the Ceq
1. Use the shift method we can decrease the couple between lines and can increase self-resonance frequency, but the Q is down.
2. Use metal-1 will gain the substrate resistance and capacitance.
Symmetric Inductor

With center-tapped inductor

Without center-tapped inductor
Differential Symmetric Inductor
Single-Ended vs. Differential

**Single-ended excitation**

**Differential excitation**
Single-Ended vs. Differential

At lower frequencies, $Q_L$ dominates in both cases and the Q factor increase for increasing frequency.
At higher frequencies, $R_L$ is increasing and $R_p$ is decreasing, so the $Q_d$ is larger than the $Q_{se}$.

\[
\frac{Q_d}{Q_{se}} = \frac{2R_p || R_L}{R_p || R_L} \\
\text{where } R_L = r(1 + Q_L^2)
\]
Single-Ended vs. Differential

Single-ended Q factor

Differential Q factor
Variation Process with Temperature

Q is decreasing with increasing of temperature
Crossed-Coupled Oscillator

The condition of the loop oscillates

\[ g_{m1} R_p g_{m2} R_p \geq 1 \]
Symmetric Inductor
Symmetric Inductor
Surrounding Ground Shield (SGS)
Patterned Ground Shield (PGS)
Cross section of an inductor based on Si 3-D MMIC technology.
RF spice models
(1) THE BSIM3 MOS diode mode is disabled by setting AS, AD, PS and PD to zero.

(2) THE value of overlap capacitance of the BSIM3 MOS model are re-adjusted to fit the RF characteristics.

In addition, the following passive elements are added:

(1) $R_{bulk1}$, $R_{bulk2}$, and $R_{bulk3}$ to model the substrate resistance.
(2) $R_{gate}$ to model the gate resistance.
(3) Drain/Source to bulk junction diodes.
(4) Proximity capacitance & its associated high frequency resistance.
(5) Parasitic resistance connected to the drain/source of MOS transistor.
<table>
<thead>
<tr>
<th>MIN*</th>
<th>25 x 25(μm²)</th>
<th>50 x 50(μm²)</th>
<th>100 x 100(μm²)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cs(pF)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rs(Ω)</td>
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</tr>
<tr>
<td>Ls(pH)</td>
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<td></td>
<td></td>
</tr>
<tr>
<td>Cp(fF)</td>
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<td></td>
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</tr>
<tr>
<td>Rp(Ω)</td>
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<tr>
<td>E11(%)</td>
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<tr>
<td>E21(%)</td>
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<tr>
<td>E22(%)</td>
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<tr>
<td>E12(%)</td>
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<tr>
<td>Fr(GHz)</td>
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<td></td>
<td></td>
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<tr>
<td>Q(1GHz)</td>
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</tbody>
</table>

* : Area calculated from Ltop
Total gate width (Wg) = Lf \times N

Finger length, \( L_f \)
$L_{top} : \text{Top plate metal edge}; \ 25\mu m \leq L_{top} \leq 100\mu m$

$L_{bot} : \text{Bottom plate metal edge}; \ L_{bot} = L_{top} + 2 \times 5\mu m$
The RF model is characterized at the following bias range:

- 2.5V NMOS
- 2.5V PMOS
- 3.3V NMOS
- 3.3V PMOS

Where

\[
\begin{align*}
R_s (\Omega) & : \\
L_s (\mu H) & : \\
C_s (\mu F) & : \\
C_p (\mu F) & : \\
R_p (\Omega) & : \\
\end{align*}
\]

\[L_{\text{top}} = \text{edge per side of top plate metal in } \mu \text{m}\]

\[L_{\text{bot}} = \text{edge per side of bottom plate metal in } \mu \text{m}\]
Structure A - Signal line with neighboring power lines:

```
  GND  space  signal  space  GND
```

Structure B - Signal line with neighboring power lines:

```
  GND  space  signal  space  GND
```

GND
<table>
<thead>
<tr>
<th>Ls (nH)</th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Rs (Ω)</td>
<td></td>
</tr>
<tr>
<td>Cs (fF)</td>
<td></td>
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<tr>
<td>Cox1 (fF)</td>
<td></td>
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<tr>
<td>Cox2 (fF)</td>
<td></td>
</tr>
<tr>
<td>Rsub1,2 (Ω)</td>
<td></td>
</tr>
<tr>
<td>Csub1,2 (fF)</td>
<td></td>
</tr>
<tr>
<td>Elements</td>
<td>Scaling rule</td>
</tr>
<tr>
<td>---------</td>
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</tr>
<tr>
<td>MOS</td>
<td></td>
</tr>
<tr>
<td>$R_g(\Omega)$</td>
<td></td>
</tr>
<tr>
<td>$R_d(\Omega)$</td>
<td></td>
</tr>
<tr>
<td>$R_s(\Omega)$</td>
<td></td>
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<tr>
<td>$C_{ds}(fF)$</td>
<td></td>
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<tr>
<td>$R_{ds}(\Omega)$</td>
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<td>$C_{db}(fF/\mu m^2)$</td>
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<td>$C_{sb}(fF/\mu m^2)$</td>
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<td>$R_{bulk1}(\Omega)$</td>
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<td>$R_{bulk2}(\Omega)$</td>
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<tr>
<td>$R_{bulk3}(\Omega)$</td>
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</tbody>
</table>

*L, XL, Lint with unit in um*
<table>
<thead>
<tr>
<th>Elements</th>
<th>Scaling rule</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOS</td>
<td></td>
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<tr>
<td>$R_g(\Omega)$</td>
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<td>$R_d(\Omega)$</td>
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<td>$R_s(\Omega)$</td>
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<tr>
<td>$C_{ds}(fF)$</td>
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<td>$R_{bulk1}(\Omega)$</td>
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<td>$R_{bulk3}(\Omega)$</td>
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<td></td>
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<td>$R_{bulk1}(\Omega)$</td>
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<td>$R_{bulk2}(\Omega)$</td>
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<tr>
<td>$R_{bulk3}(\Omega)$</td>
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</tr>
<tr>
<td>Elements</td>
<td>Scaling rule</td>
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<tr>
<td>MOS</td>
<td></td>
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<tr>
<td>Rg(Ω)</td>
<td></td>
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<tr>
<td>Rd(Ω)</td>
<td></td>
</tr>
<tr>
<td>Rs(Ω)</td>
<td></td>
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<tr>
<td>Cds(FF)</td>
<td></td>
</tr>
<tr>
<td>Rds(Ω)</td>
<td></td>
</tr>
<tr>
<td>Cdb(FF/um²)</td>
<td></td>
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<tr>
<td>Csb(FF/um²)</td>
<td></td>
</tr>
<tr>
<td>Rbulk1(Ω)</td>
<td></td>
</tr>
<tr>
<td>Rbulk2(Ω)</td>
<td></td>
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<tr>
<td>Rbulk3(Ω)</td>
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<tr>
<td>Elements</td>
<td>Scaling rule</td>
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<td>--------------</td>
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<td>MOS</td>
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<td>$R_g(\Omega)$</td>
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<td>$R_s(\Omega)$</td>
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<td>$C_{ds}(\text{fF})$</td>
<td></td>
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<tr>
<td>$R_{ds}(\Omega)$</td>
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<td>$C_{db}(\text{fF/um}^2)$</td>
<td></td>
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<td>$C_{sb}(\text{fF/um}^2)$</td>
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<td>$R_{bulk1}(\Omega)$</td>
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<td>$R_{bulk2}(\Omega)$</td>
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<td>$R_{bulk3}(\Omega)$</td>
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<td>Elements</td>
<td>Scaling rule</td>
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<td>R_g(Ω)</td>
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<tr>
<td>C_ds(fF)</td>
<td></td>
</tr>
<tr>
<td>R_ds(Ω)</td>
<td></td>
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<td>C_db(fF/um²)</td>
<td></td>
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<td>C_sb(fF/um²)</td>
<td></td>
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<td>R_bulk1(Ω)</td>
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<td>R_bulk2(Ω)</td>
<td></td>
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<tr>
<td>R_bulk3(Ω)</td>
<td></td>
</tr>
<tr>
<td>N</td>
<td>Rsub1 (Ohm)</td>
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<tr>
<td>----</td>
<td>-------------</td>
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<tr>
<td>6.5</td>
<td></td>
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<tr>
<td>5.5</td>
<td></td>
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<tr>
<td>4.5</td>
<td></td>
</tr>
<tr>
<td>3.5</td>
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<tr>
<td>2.5</td>
<td></td>
</tr>
</tbody>
</table>
N : number of the coil turns, which is 2.5 in the example of fig.

W : width of top metal.

S : space of top metal.

R : radius of inner coil.
<table>
<thead>
<tr>
<th>Structure</th>
<th>(as drawn)</th>
<th>(after process bias)</th>
</tr>
</thead>
<tbody>
<tr>
<td>M1-PO1-FOX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M2-PO1-FOX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M3-PO1-FOX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M4-PO1-FOX</td>
<td></td>
<td></td>
</tr>
<tr>
<td>M5-PO1-FOX</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Typical Interconnect Capacitance Table**

**********Structure B**********
### TYPEICAL INTERCONNECT CAPACITANCE TALBE

<table>
<thead>
<tr>
<th>Structure</th>
<th>(as drawn) width</th>
<th>space</th>
<th>(after process bias) width</th>
<th>space</th>
<th>Ctotal</th>
<th>Cc</th>
<th>Cbottom</th>
<th>Ca</th>
<th>Cf</th>
<th>Csum/Ctotal</th>
</tr>
</thead>
<tbody>
<tr>
<td>PO1-FOX</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>8x10x0.24</td>
<td>16x10x0.24</td>
<td>8x10x0.34</td>
<td>16x10x0.5</td>
<td>32x10x0.24</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>---</td>
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<td>------------</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rg(Ω)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rd(Ω)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rs(Ω)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cds(fF)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rds(Ω)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rbulk1(Ω)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Rbulk3(Ω)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E11(%)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E21(%)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E22(%)</td>
<td></td>
<td></td>
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<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E12(%)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Mean(%)</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>E12 calculated start from 1GHz</td>
<td>Mean(%)</td>
<td>E12(%)</td>
<td>E22(%)</td>
<td>E21(%)</td>
<td>Rbulk1(Ω)</td>
<td>Rbulk2(Ω)</td>
<td>Rds(Ω)</td>
<td>Rd(Ω)</td>
<td>Rg(Ω)</td>
<td></td>
</tr>
<tr>
<td>--------------------------------</td>
<td>---------</td>
<td>--------</td>
<td>--------</td>
<td>--------</td>
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<td></td>
</tr>
<tr>
<td></td>
<td>8×10^0.24</td>
<td>16×10^0.24</td>
<td>8×10^0.34</td>
<td>16×10^0.5</td>
<td>32×10^0.24</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Chapter 9  Latch-up

- Principles of CMOS Latch-up
- Latch-up Trigger Sources in CMOS IC’s
- Latch-up Prevention
- Layout Spacing in Scaled-Down
- CMOS Process Guard Rings Layout
- Cell Layout to Increase Latch-up Immunity
- Latch-up Prevention in I/O Cells
Principles of CMOS Latch-up
Guard Ring Layout Step

(1) inverter

(2) Thin oxide

(3) P+ implement
Guard Ring Layout Step

(4) N+ implement

(5) contact

(6) metal 1
Double Guard Ring Layout

For some special devices, ex: bipolar, diode, resister; charge pump, high noise or high power, can use double guard ring or triple guard ring.
Double Guard Ring Layout Step

1. Inverter
2. Thin oxide
3. P+ implement
Double Guard Ring Layout Step

(4) N+ implement

(5) Contact

(6) Metal 1
Triple Guard Ring Layout Step

(1) Thin oxide
(2) p+ implement
(3) N-Well
Triple Guard Ring Layout Step

(4) Contact

(5) Metal 1

(6) Thin oxide
Triple Guard Ring Layout Step

(7) N+ implement

(8) P+ implement
Triple Guard Ring Layout Step

(9) contact

(10) Metal 1

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Latch-up Prevention in CMOS IC
Latch-up Trigger Source in CMOS IC

![Diagram of Latch-up Trigger Source in CMOS IC](image)
Latch-up Trigger Source in CMOS IC (cont’d)
Latch-up Prevention by Increasing Holding Voltage

\[ V_{\text{hold}} = V_{\text{DD}} - V_{\text{SS}} = V_{\text{ce}} + I_sR_s + V_{\text{been}} = V_{\text{ce}} + (I_s + I_{\text{bn}})R_s + I_sR_{\text{sub}} = V_{\text{ce}} + V_b \cdot n^* (1 + R_s/R_{\text{sub}}) \]

To increase \( V_{\text{hold}} \) -> increase \( R_s \)
or
\( R_w, \text{or Reduce } R_{\text{well}} \text{ or } R_{\text{sub}} \)
Latch-up Prevention by Epitaxial Substrate

![Diagram showing the structure of an epitaxial substrate with labeled components: VDD, Vss, N+, P+, Rwell, N-well, P-Epi-layer, P+ sub, Rsub, and thickness. The diagram also includes a graph illustrating the relationship between HODING voltage and N+ to P+ separation in microns for different epitaxial thicknesses (3um EPI material implanted n-well, 5um EPI material diffused n-well, and 12um EPI material diffused n-well).]
Latch-up Prevention by Retrograde Well
Latch-up Prevention by Trench Isolation

![Diagram showing Latch-up Prevention by Trench Isolation]
Guard Rings to Prevent Latch-up in the Output Cell
Layout Spacing in Scaled-Down CMOS Process

VDD  
N-well  
P-sub  
Latchup Path  
X  
Y  

VSS  

VDD  
N-well  
P-sub  

VSS
Cell Layout of the Internal Circuit

Typical Cell Layout

Cell Layout with Guard Ring

This p-n-p-n path is sensitive to latchup issue

Occupy more layout area

Guard Ring
Reduce Contact to Increase Latchup Immunity

The original layout

The modified layout

Theory

VDD

Rwell

Rp

Rn

Rsub

VSS

VSS

VDD
Critical Spacings for Latchup Prevention

- **Spacing 1**: Between P+ and N+ regions.
- **Spacing 2**: Between P+ and P+ regions.
- **N-well**: Represents the diffusion region for n-type impurities.
- **P-sub**: Represents the diffusion region for p-type impurities.
- **VDD**: Positive power supply.
- **VSS**: Negative power supply.
- **Rwell**: Well resistance.
- **VEB**: Emitter-base voltage.
- **VBE**: Base-emitter voltage.
- **Rsub**: Substrate resistance.
- **Itrig**: Trigger current.
Efficient Methodology to Extract Compact Layout Rules for Latchup Prevention in the Internal Circuit
Additional Guard Rings to Prevent Latchup Occurrence in the Internal Circuit due to IO Pad Triggering
Critical Spacing for Latchup Prevention in I/O Cells

The output buffer should be latchup-free
Layout of the Instance for Connection from the Power Lines to the Guard Rings

(a) a single metal layer:

(b) multiple metal layers:
   (but forbidden VIA stack)
Method to Automatic Place the Guard Rings at the Selected Layout Regions

(a) The location to be added the additional guard rings
(b) The diffusion region is added under the power line

(c) The guard ring connection is formed by the instance method
(d) The guard ring connection is formed by the mosaic method
Method to Automatically Place the Guard Rings at the Selected Layout Regions (cont’d)

The layout (a) before, and (b) after, adding the guard ring under the power line by the Guard Ring Automation program.

(a) Before

(b) After
Flowchart of the Guard Ring Automation Program

1. Create pull-down menu in OPUS
2. Under select the guard ring & choose to create VDD or VSS ring
3. Determine the process & get the library
4. Get the latname, size, & position of guard ring
5. Get the correct instance from library
6. Create nwell, implant, & diffusion on guard ring by design rule
7. Find all of the metal layer which was overlap the guard ring
8. Create temp layers on the guard ring
9. Chop the temp layer according to the signal & PG metal lines
10. Get the temp layer & determine the shape
11. Calculate the size of mosaic & put cells on the temp layer with mosaic type by design rule
12. Use the correct metal layer instead of the temp layer
13. Erase unnecessary metal & temp layers
14. Merge all metal, nwell, implant, & diffusion
15. Put the most cells on the temp layer with single instance type by design rule
16. DONE
Chapter 10 ESD (Electrostatic Discharge)

- Resistor
- Diode
- MOS Device
- Silicon Controlled Rectifier (SCR)
- Parasitic Devices
ESD Design Rule

1. ESD = electrostatic discharge protection
2. ESD NMOS and PMOS should have a non-salicide area on drain side, that is PRO mask should block drain side of device.
3. Contact and vias should be used as many as possible
4. Metal lines in ESD discharge path should follow 45 degree corner
ESD Test Method

1. HBM : Human Body Model
2. MM : Machine Model
3. CDM : Charge Device Model
ESD Layout
Cross Section of ESD Device
<table>
<thead>
<tr>
<th>ESD Design Rule</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min. total finger width for ESD NMOS/PMOS</td>
</tr>
<tr>
<td>The min. width of PRO on drain side and PRO edge for 2.5v NMOS without ESD implant</td>
</tr>
<tr>
<td>The min. width of PRO on drain side and PRO edge for 2.5v PMOS</td>
</tr>
<tr>
<td>The min. clearance of poly edge to CO edge on source side for NMOS and PMOS</td>
</tr>
<tr>
<td>Min. gate length of NMOS without ESD imp.</td>
</tr>
<tr>
<td>Min. gate length of PMOS no ESD imp</td>
</tr>
<tr>
<td>Min. width of metal lin connecting bond pad and protection device</td>
</tr>
<tr>
<td>Min. vss and vdd power ring metal width</td>
</tr>
<tr>
<td>Min. metal width on drain side of ESD device</td>
</tr>
</tbody>
</table>
ESD Layout

- Substrate
- Source
- Drain
- P+
- ESD imp
- RPO
Silicided-Diffusion Blocking Region
Salicide Block (SAB) Mask For ESD Protection
Layout Without Using Silicided-Blocking Mask
N-well Resistor
**N+ Diffusion Resistor w/ i Silicide Block**

- **n+ diffusion resistor**
- **n+ diffusion resistor w/ silicide block**
Polysilicon Resistor
Single Finger P+ Diode
Two-Finger P+ Diode
Three-Finger P+ Diode
N+ Diode Structure
N-well Diode Structure

P+ Anode

N-Well Cathod

P+Anode

N-well Cathod

P+ N+
Non-Gated Thick Oxide Well to Well Device
Gated Thick Oxide Well to Well Device
Non-Gated Thick Oxide N+ to N-well Device
Gated Thick Oxide N+ to N-well Device
Gated Thick Oxide N+ to N+ Device
Single Finger N-Channel MOSFET
Multi-Finger N-Channel MOSFET
N-Channel MOSFET with Integrated N-well Resistor
Single Finger P-Channel MOSFET
Multi Finger P-Channel MOSFET

Source

Drain

TF GATE

Antenna Diffusion

Source

Antenna Diffusion

Drain

N+ P+ P+ P+

N-well
Multi Finger PMOS with Local Well Trap
Thick Oxide NPN Triggered SCR

CATHODE

ANODE

CATHODE

ANODE

P+  N+  N+  P+  N+

N-well
Low-Voltage NMOS Triggered SCR
Finger-Type Layout of CMOS Devices for ESD
The Effect of Silicide-Blocking (RPO)
Muti Finger MOSFET Under Different Layout Direction

Vertical type (poly to power line)

Horizontal type (poly to power line)
Finger-Type Layout of ESD Protection NMOS
Equivalent Circuit of the ESD Protection NMOS
Finger-Type Layout of ESD Protection NMOS
Finger-Type Layout of ESD-Protection NMOS with Equal Substrate Resistance

PAD

Rsub

Rsub

Rsub

Rsub
NPN (PNP) Structure of the NMOS (PMOS)
Muti Finger with Different Numbers of Additional Pick-up Called NPN(PNP) Structure

(a) NPN(PNP) = 0
(b) NPN(PNP) = 1
(c) NPN(PNP) = 2
(d) NPN(PNP) = 4
Design Rules on NPN(PNP) Structure of the NMOS
New Layout Style of I/O NMOS (PMOS) to Improve Uniform Turn-on Behavior
Layout Style to Realize a Large-size Output NMOS(PMOS) with Multiple-Fingers & Uniform Turn-on Behavior
**Lateral SCR (LSCR) Device**

**Diagram Details:**
- **Input pad** connected to **IESD**.
- **N-Well** and **P+** regions highlighted.
- **Von** = \( (It2 \times R + Vt2) \)
- **Holding region** and **Trigger point** (\( \sim 50V, \sim 10mA \))
- **VDD** and **VSS** connections indicated.
Modified Lateral SCR (MLSCR) Device

\[
\text{Von} < (I_t \times R + V_{t2})
\]
Low-Voltage-Trigger Lateral SCR (LVTSCR) Device
Gate-Coupled LVTSCR

Diagram showing the gate-coupled LVTSCR circuit with components labeled and connected.
Device Structure in High-Voltage CMOS Process

Asymmetric HV NMOS (both Drain can sustain HV)

S  D

N+  N+  NDD

NLDD  NDD  P-sub
Device Structure in High-Voltage CMOS Process (symmetric)

Symmetric HV NMOS (both Drain/Sorce can sustain HV)

S

D

N+/p+ N+/p+
NDD/PDD NDD/PDD

P-sub

NDD/PDD

N+/P+
HV-NMOS Structure in 40v CMOS Process

Asymmetric HV NMOS
(only Drain can sustain HV)

S

D

N+
P-well

FOX

HVNW

P-sub

OD1

OD2

HVNW

N+

S

D
**HV-Pmos Structure in 40v CMOS Process**

Asymmetric HV NMOS
(only Drain can sustain HV)

- S
- D

- N+ P+ P+
- N-well HVPW N-well
- NBL (N+ Buried Layer)
- P-sub

- OD1
- OD2
- HVPW

- P+ N-well

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The N-channel ESD Device Proposed in TSMC 1.0-u 16v High CMOS Process
Cross-Sectional of Gate-Grounded NMOS (ggNMOS) for ESD Protection
Traditional Bond Pad

- Bond wire
- Multi-metal layers
- Via 3-4
- Via 2-3
- Via 1-2
- CMeq
- P-sub
Low Capacitance Bond Pad

Multi-metal layers

Insert additional diffusion layer (serial capacitance)

Reduce capacitance to 30% of the traditional bond pad

Parasitic capacitance

Cp

Cn

P-sub

N-well

P+

Via 1-2

Via 2-3

Via 3-4

CMeq

Bond wire
Low-Capacitance Bond Pad with Good Bonding Reliability

Multi-metal layers

Wire bonding platter (better adhesion)

Insert additional diffusion layer (serial capacitance)

Parasitic capacitance
Chapter 11  Analog Cells/Macros Layout

- Amplifiers Layout
- MOS Switches
Two-Stage OTA
Mirrored Cascode OTA

(a)

(b)

VDD

M10 M11 M12 M13

IN- M1 M2 IN+

VB2 M3

M4

M5 M6

VB1 M9

M8

VSS

M4 M4 M4 M10 M11 M12 M13

M1 M2 M2 M1 M1 M2 M2 M1 M1

M5 M5 M5 M7 M9 M9 M8 M6 M6

M6 M6

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Folded Cascode OTA

(a)

(b)
Common-Centroid Layout

```
<table>
<thead>
<tr>
<th>n1</th>
<th>n2</th>
<th>n1a</th>
<th>n2a</th>
</tr>
</thead>
<tbody>
<tr>
<td>n2</td>
<td>n1</td>
<td>n2a</td>
<td>n1a</td>
</tr>
<tr>
<td>n3</td>
<td>n3</td>
<td>n30</td>
<td>n30</td>
</tr>
<tr>
<td>sn3</td>
<td>sn30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>sp3</td>
<td>sp30</td>
<td></td>
<td></td>
</tr>
<tr>
<td>p3</td>
<td>p3</td>
<td>p30</td>
<td>p30</td>
</tr>
<tr>
<td>p2</td>
<td>p1</td>
<td>p2a</td>
<td>p1a</td>
</tr>
<tr>
<td>p1</td>
<td>p2</td>
<td>p1a</td>
<td>p2a</td>
</tr>
</tbody>
</table>
```
Interdigitized Layout

![Interdigitized Layout Diagram]
Interdigitized Layout
Interdigitized Layout
Layout of Differential Pair OP Amplifier Example
Layout of Differential Pair OP Amplifier Example

Case 1

Case 2

Case 3
Layout of Differential Pair

- Input stage M1&M2, common centroid to reduce offset, don’t use minimum size for process variation.

- M3&M4, symmetric, same orientation.

- No signal crossing allowed between M1&M3, M2&M4.

- Node N2 can only use metal wire as short as possible, avoid crossing.

- Capacitor layout in Well connected to independent power line not sharing with OP power line independent well to M5 and M7 to avoid noise.

- Substrate of M1&M2 connected to N1 ( triple well required ), not the power line.

- Keep input and output nodes away, put the capacitor between them.

- Put the capacitor between M6 and M7 ( case3 ), to avoid latch up.
**Layout of Differential Pair**

- Output node connected to capacitor bottom plate to avoid the substrate noise coupled to input stage and be amplified.

- Don’t cross input and output wire to avoid feedback oscillation.

- Keep drain nodes of MOS as small as possible to reduce the output capacitance.

- Divide the compensation capacitor into multiple units to avoid antenna effect.
Switch

- Use Minimum of area transistor whenever possible
- Minimize parasitic capacitance between substrate and drain/source
- Limiting coupling through substrate of digital and analog parts.
- Avoid crossing analog signals with digital signals.
- Substrate bias separates the switches and the bus carrying the digital signals defines a protective guard ring
A one-stage circuit for low frequency applications
A conventional two-stage circuit.
A folded cascode circuit for high frequency applications.
Folded-Cascode
Layout for Large W/L Ratio

- **Active Area**
- **Poly1**
- **Metal**
- **Contact**

(a)  
(b)
Layout of current mirror without $\Delta W$ correction techniques.

Layout of current mirror with $\Delta W$ correction techniques.
Current Switch DAC

Worse

F*8  E*4  D*2  C  B  A*3  B  C  D*2  E*4  F*8

Better

|   | V | C |  | V | C |  | V | C |  | V | C |  | V | C |  | V | C |  |
|   | A |   |   | F | F | F | F | F | F | F | F | F | F | F | F | F | F | F |
| DUMMY | V | C | C | DUMMY | V | C | C | DUMMY | V | C | C | DUMMY | V | C | C | DUMMY | V | C | C |
|   | C |   |   | C | E | E | E | E | D | D | C | V | A | C | B | V | C | B |
| DUMMY | V | C | C | DUMMY | V | C | C | DUMMY | V | C | C | DUMMY | V | C | C | DUMMY | V | C | C |

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27
Interdigitized Layout

Interdigitized

Case 1

\[
\begin{array}{cccccc}
1 & 1 & 2 & 2 & 1 & 1 \\
\end{array}
\]

\[
\begin{array}{cccccc}
\bullet & \bullet & \bullet & \bullet & \bullet & \bullet \\
\end{array}
\]

\[
\begin{array}{cccccc}
1 & 1 & 2 & 2 \\
\end{array}
\]

Case 2

\[
\begin{array}{cccccc}
1 & 2 & 2 & 1 & 1 \\
\end{array}
\]

\[
\begin{array}{cccccc}
\bullet & \bullet & \bullet & \bullet & \bullet & \bullet \\
\end{array}
\]

\[
\begin{array}{cccccc}
2 & 2 & 1 & 1 & 2 \\
\end{array}
\]

Case 3

\[
\begin{array}{cccccc}
D & 1 & 2 & 2 & 1 \\
\end{array}
\]

\[
\begin{array}{cccccc}
\bullet & \bullet & \bullet & \bullet & \bullet & \bullet \\
\end{array}
\]

\[
\begin{array}{cccccc}
2 & 1 & 1 & 2 & D \\
\end{array}
\]

Case 4

\[
\begin{array}{cccccc}
1 & 2 & 1 & 2 & 1 & 2 \\
\end{array}
\]

\[
\begin{array}{cccccc}
\bullet & \bullet & \bullet & \bullet & \bullet & \bullet \\
\end{array}
\]

\[
\begin{array}{cccccc}
1 & 2 & 1 & 2 \\
\end{array}
\]
Chapter 12  Power Distribution and Signal-Integrity

- Electrical Consideration for IC layout
- Power Distribution
- Example of Power Analysis
- Cross Talk
- Interconnect RC Effect
- Inductance
- Number of Power Pads
- Mixed – Signal Power Distributions
1. Power Supply Planning
   ◆ influences of metal migration, IR drop, ground bounce
   ◆ understand whole chip power dissipation
   ◆ point out the macros dissipation maximum of power pads
   ◆ power line distribution, avoid disconnection of power lines
   ◆ decision of power line (pad) width from power dissipation
   ◆ using metal lines as power distribution only
   ◆ separation power lines of internal CKT & external I/O
   ◆ separation analog & digital power supply
   ◆ independent power supply for large power circuit, (macro), as close as possible
   ◆ put substrate (well) contacts as many as possible
   ◆ M1 to M2, put via as many as possible
   ◆ corner of large power line, shape & hole

Separation of power supply
   ◆ from pin
   ◆ from pod
   ◆ from power line
2. Wire loading consideration
   ◆ time delay (RC) delay
   ◆ driving capability
   ◆ optimum size of IC Layout
   ◆ find critical path & net
   ◆ P & R for critical path & net first
   ◆ set group of critical path & net
   ◆ set constraints of critical path & net
   ◆ understanding of cells driving capability & loading
   ◆ rearrangement of cell at proper position
   ◆ charge a larger driving cell
   ◆ insert buffer & reduce the wire load
   ◆ consideration of global & internal block buffer
   ◆ reduce the circuit loading driven by buffer
Electrical Consideration for IC Layout

3. Routing width determination

- improper design of line width
  - RC delay, \( R \downarrow C \uparrow \) or \( R \uparrow C \downarrow \)
  - metal migration rule, about 1mA/1um
  - increasing layout area
  - \( C \uparrow \), loading \( \uparrow \), power \( \uparrow \)

- determination from power dissipation & operating current
Electrical Consideration for IC Layout

4. Resistance & Capacitance
   - increasing performance, accuracy
   - area efficient
   - noise immunity
   - $R$: metal, poly, N+, P+, well
   - $C$: poly-2/poly-1, metal-1/poly-1, MOS, MiM
   - $n^+$, $P^+$, well, MOS, junction bias dependent

Guides:
   - width of $R$ cannot be too narrow
   - planning of unit $R$ & unit $C$
   - put contacts as many as possible at source/drain area
   - $R$ & $C$ element cannot be crossover by other interconnections
5. **Clock skew & race**
   - point out the critical path
   - design clock tree, synthesis design & path of cell by hand
   - arrangement of module in P & R
   - set cell group in P & R
   - set critical constraints in P & R
   - turning of clock timing to each module
   - layout matching
   - set critical module as a macro

6. **Noise consideration**
   - coupling (cross talk) noise
   - ground bounce
   - high frequency, low frequency
   - avoid long parallel distribution
   - isolation by clean power supply
   - separation of analog & digital signal
   - shielding, guard ring
Digital/Analog Power Lines

a

b

c

d

e

f

POWER
PAD
DIGITAL
ANALOG
PAD
POWER

POWER
PAD
DIGITAL
ANALOG
PAD
POWER

POWER
PAD
DIGITAL
ANALOG
PAD
POWER
Metal Layers and Power Distribution

21064

Metal 3
Metal 2
Metal 1

21164

Metal 4
Metal 3
Metal 2
Metal 1

21264

RP2/Vdd
Metal 4
Metal 3
RP1/Vss
Metal 2
Metal 1
Fingers Power Distributions

An example of cross section

An example top layer
Two Layer Grid Power Distributions

- **VDD**
- **GND**

1st layer

2nd layer

Contact cuts
Routing Cell-Based IC

- Cell height
- Feed though
- Channel routing
- Power lines

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Area vs. IR Drop Balance

Block A

Block B

Block A

Block B
Design of an Efficient Power Distribution Network for the UltraSPARC-I Microprocessor

Hong-Yi Huang 黃弘一

UltraSPARC-I floorplan grouping
Power distribution network for control block
Effect of power-line resistance on on-chip coupling noise

a=0, b=1 → 0

Discharging current through Rs affects node a
## Result of scaling theories in conventional MOS technology

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Constant Field</th>
<th>Constant Voltage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device Dimensions</td>
<td>$\alpha^{-1}$</td>
<td>$\alpha^{-1}$</td>
</tr>
<tr>
<td>Chip Size</td>
<td>$\alpha^{0}$</td>
<td>$\alpha^{0}$</td>
</tr>
<tr>
<td>Pad Size</td>
<td>$\alpha^{0}$</td>
<td>$\alpha^{0}$</td>
</tr>
<tr>
<td>Number of Devices</td>
<td>$\alpha^{2}$</td>
<td>$\alpha^{2}$</td>
</tr>
<tr>
<td>Voltage</td>
<td>$\alpha^{-1}$</td>
<td>$\alpha^{0}$</td>
</tr>
<tr>
<td>Current / Device</td>
<td>$\alpha^{-1}$</td>
<td>$\alpha^{1}$</td>
</tr>
<tr>
<td>Current / Chip</td>
<td>$\alpha^{1}$</td>
<td>$\alpha^{3}$</td>
</tr>
<tr>
<td>Gate Oxide Thickness</td>
<td>$\alpha^{-1}$</td>
<td>$\alpha^{-1}$</td>
</tr>
<tr>
<td>Height of Metal</td>
<td>$\alpha^{-1}$</td>
<td>$\alpha^{-1}$</td>
</tr>
<tr>
<td>Resistance of Metal</td>
<td>$\alpha^{1}$</td>
<td>$\alpha^{1}$</td>
</tr>
<tr>
<td>Current Density</td>
<td>$\alpha^{2}$</td>
<td>$\alpha^{4}$</td>
</tr>
<tr>
<td>Power Line Voltage Drop</td>
<td>$\alpha^{2}$</td>
<td>$\alpha^{4}$</td>
</tr>
<tr>
<td>Signal / Noise Ratio</td>
<td>$\alpha^{-3}$</td>
<td>$\alpha^{-4}$</td>
</tr>
</tbody>
</table>
Design flow of robust routed power distribution for low power ASIC

Example objective ------ to minimize the area of the power and ground networks for several given constraints such as IR drop and EM.

Typically the routed power distribution is designed hierarchically, first at the local block, then at the global level to satisfy reliability and noise tolerance.
Local power distribution network design methodology

- Checking Logic & Timing SW Activity Factor
- Sizing Driver
- Modeling Inputs

Simulation

- Peak (Noise)
- RMS (Joule heating)
- Average (EM)

SPEC
- Yes
  - End
- No
  - Split Length or Widen Width
The currents can be measured precisely by circuit simulation. The peak, average, and RMS currents are necessary to calculate the IR drop, EM, and Joule heating respectively. Power bus line widths are determined based on these measured currents.
Global power distribution network design methodology
Maximum IR Drop

\[ \sum_{i \in U} \rho_i \frac{L_i}{W_i} \leq v_{\text{max}} \]

\( U \): the total paths from power pad to FUB terminals

Maximum Noise from L di/dt

\[ V_{n_{\text{max}}} = L \frac{I_p}{t_a} = L \left( 2 \frac{C_{\text{sw}} V_{\text{sw}}}{t_f} \right) \frac{1}{t_a} \]

\[ V_{n_{\text{max}}} = \frac{V_{\text{dd}} C_{\text{sw}}/2}{2C_d + C_{\text{sw}} + t_f^2/6L} \]
EM Widths

\[ W = \frac{P_{\text{tot}}}{T_{J_{\text{max}}} V_{\text{DD}}} \]

Joule Heating Effect

\[ T_{\text{TF}} = Aj^{-n} \exp \left( \frac{Q}{K_B T_m} \right) \]

\[ \Delta T_{\text{selfheating}} = I_{\text{rms}}^2 RR_{\theta} \]
Details of possible power routing strategies in control block
Cross Talk

Line-to-line parasitic capacitance $C_m$
Mutual inductance $L_m$
- Troublesome problem in high-density layout
- Incorrect or false transition may occur.
Cross Talk

\[ Q_1 = C_{11}V_1 + C_{12}(V_1 - V_2) \]
\[ Q_2 = C_{21}(V_2 - V_1) + C_{22}V_2 \]
\[ \Phi_1 = L_{11}I_1 + L_{12}I_2 \]
\[ \Phi_2 = L_{21}I_1 + L_{22}I_2 \]

I = \frac{dQ}{dt} \quad C_m = C_{12} = C_{21} \quad V = \frac{d\Phi}{dt} \quad L_m = L_{12} = L_{21}

I_1 = C_{11} \frac{dV_1}{dt} + C_m \frac{d(V_1 - V_2)}{dt}
I_2 = C_m \frac{d(V_2 - V_1)}{dt} + C_{22} \frac{dV_2}{dt}
V_1 = L_{11} \frac{dl_1}{dt} + L_m \frac{dl_2}{dt}
V_2 = L_m \frac{dl_1}{dt} + L_{22} \frac{dl_2}{dt}
Hazards (glitches) appear on the interconnects due to coupling effects. According to the high noise immunity capability, the hazards disappear after the CMOS static circuits.
RLCG Interconnect Tree

Voltage $V_A$

- $\tau_{delay}$
- $\tau_{buffer} + \tau_{flight}$
- $\tau_{rise}$
- $\tau_{settle}$

Voltage $V_B$

- $\tau_{delay}$

Time
Interconnect Delay in Deep Submicron Technology

![Graph 1: Wire Length/Chip Diagonal Length vs. Probability](image1)

- **Intra-module connections**
- **Inter-module connections**

![Graph 2: Delay (ns) vs. Minimum Feature Size](image2)

- **Typical gate delay**
- **Interconnect gate delay**

Hong-Yi Huang 黃弘一
## Summary of Interconnect R and C Parameters

<table>
<thead>
<tr>
<th>Min. wire width (μm)</th>
<th>Min. wire space (μm)</th>
<th>10000 μm metal-1 wire</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>R</td>
</tr>
<tr>
<td>0.35 μm</td>
<td>0.5</td>
<td>1.7kΩ</td>
</tr>
<tr>
<td>0.25 μm</td>
<td>0.32</td>
<td>2.38kΩ</td>
</tr>
<tr>
<td>0.18 μm</td>
<td>0.23</td>
<td>3.39kΩ</td>
</tr>
</tbody>
</table>

Hong-Yi Huang 黃弘一
Lumped RC Model

\[ V_{out}(t) = V_{DD}(1 - e^{-t/RC}) \]

output reach 50% point at \( t = t_{PLH} \)

\[ V_{50\%} = V_{DD}(1 - e^{-t_{PLH}/RC}) \]

\[ t_{PLH} = 0.69RC \]

RC Delay Model

Distributed RC Ladder Network
Elmore Delay Model

at node 7

\[ t_{D7} = R_1(C_1+C_2+C_3+C_4+C_5) + (R_1+R_6)C_6 + (R_1+R_6+R_7)C_7 + (R_1+R_6+R_7+R_8)C_8 \]

at node 5

\[ t_{D7} = R_1(C_6+C_7+C_8) + R_1C_1 + (R_1+R_2)C_2 + (R_1+R_2+R_3)C_3 + (R_1+R_2+R_4)C_4 + (R_1+R_2+R_4+R_5)C_5 \]
**Distributed RC Effect**

\[ C \frac{dV_i}{dt} = (I_{j-1} - I_j) = \frac{(V_{j-1} - V_j)}{R} - \frac{(V_j - V_{j+1})}{R} \]

\[ rc \frac{dV}{dt} = \frac{d^2V}{dx^2} \]

\[ tx = k \cdot x^2 \]

\[ tl = \frac{(rc \cdot l^2)}{2} \]

- \( x \) = distance from input
- \( r \) = resistance per unit length
- \( c \) = capacitance per unit length
- \( tx \) = propagation delay
- \( l \) = length of wire
- \( r \) = resistance per unit length
- \( c \) = capacitance per unit length
Buffer Insertion of Long Poly Line

When RC delay of a long poly wire is high
- double metal layer, the 2nd metal replace poly
- poly still used for local gate connection
- silicide poly (2-4 Ω/□)
- important for memory word line design

For long metal line, buffer insertion required for
wire delay $\tau_w \gg$ gate delay $\tau_g$
wire length $l \gg (2 \tau_g/rc)^{1/2}$
Signal Integrity

- RC effect
- electromigration
- line-to-line coupling
Buffer Insertion

Narrow width: minimum area layout
Wide width: R ↓, C ↑, RC ↓
Buffer insertion: no wide line required
C ↓ (lower power)
RC ↓ (higher speed)
Simulation of Interconnect RC Delay

<table>
<thead>
<tr>
<th>Process</th>
<th>NMOS width</th>
<th>PMOS width</th>
<th>NMOS width</th>
<th>PMOS width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.35 μm (3.3v)</td>
<td>(0.9 n) μm</td>
<td>(2.7 n) μm</td>
<td>0.9 μm</td>
<td>2.7 μm</td>
</tr>
<tr>
<td>0.25 μm (2.5v)</td>
<td>(0.6 n) μm</td>
<td>(1.8 n) μm</td>
<td>0.6 μm</td>
<td>1.8 μm</td>
</tr>
<tr>
<td>0.18 μm (1.8v)</td>
<td>(0.5 n) μm</td>
<td>(1.5 n) μm</td>
<td>0.5 μm</td>
<td>1.5 μm</td>
</tr>
</tbody>
</table>

n=1, 2, 3, ..., 15 n: sizing ratio of inverter
Simulation Results (Different Driver Sizes)

0.35 μm process

0.25 μm process

0.18 μm process

Delay time (In to OUT)
## Driver/Receiver Sizes for Different Interconnect Length

<table>
<thead>
<tr>
<th>Process</th>
<th>NMOS width</th>
<th>PMOS width</th>
<th>NMOS width</th>
<th>PMOS width</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.35 ( \mu \text{m} ) (3.3v)</td>
<td>4.5 ( \mu \text{m} )</td>
<td>13.5 ( \mu \text{m} )</td>
<td>0.9 ( \mu \text{m} )</td>
<td>2.7 ( \mu \text{m} )</td>
</tr>
<tr>
<td>0.25 ( \mu \text{m} ) (2.5v)</td>
<td>3.0 ( \mu \text{m} )</td>
<td>9.0 ( \mu \text{m} )</td>
<td>0.6 ( \mu \text{m} )</td>
<td>1.8 ( \mu \text{m} )</td>
</tr>
<tr>
<td>0.18 ( \mu \text{m} ) (1.8v)</td>
<td>2.5 ( \mu \text{m} )</td>
<td>7.5 ( \mu \text{m} )</td>
<td>0.5 ( \mu \text{m} )</td>
<td>1.5 ( \mu \text{m} )</td>
</tr>
</tbody>
</table>
Simulation Results (Different Interconnect Length)

- **0.35 μm process**
- **0.25 μm process**
- **0.18 μm process**

Delay time vs. Wire length (μm)

- **t1**, **t2**, **t3**
Interconnect Cross Coupling Simulation Model
## Interconnect Cross Coupling Simulation Model

<table>
<thead>
<tr>
<th></th>
<th>(R \ (\Omega/\mu\text{m}))</th>
<th>(C_c \ (\text{fF/\mu m}))</th>
<th>(C_g \ (\text{fF/\mu m}))</th>
<th>(C_s \ (\text{fF/\mu m}))</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.35(\mu) m (3.3v)</td>
<td>0.17</td>
<td>0.08</td>
<td>0.07</td>
<td>0.14</td>
</tr>
<tr>
<td>0.25(\mu) m (2.5v)</td>
<td>0.24</td>
<td>0.09</td>
<td>0.05</td>
<td>0.14</td>
</tr>
<tr>
<td>0.18(\mu) m (1.8v)</td>
<td>0.34</td>
<td>0.10</td>
<td>0.04</td>
<td>0.14</td>
</tr>
</tbody>
</table>

The diagram illustrates the cross coupling model between metal layers, indicating the width, space, and height dimensions.
### Simulation of Interconnect Cross Coupling (0.35 um)

<table>
<thead>
<tr>
<th>In</th>
<th>InL, InR</th>
<th>2000um</th>
<th>4000um</th>
<th>6000um</th>
<th>8000um</th>
<th>10000um</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>R, R</td>
<td>0.32</td>
<td>0.65</td>
<td>0.92</td>
<td>1.16</td>
<td>1.52</td>
</tr>
<tr>
<td></td>
<td>R, -</td>
<td>0.36</td>
<td>0.80</td>
<td>1.12</td>
<td>1.54</td>
<td>1.89</td>
</tr>
<tr>
<td></td>
<td>R, F</td>
<td>0.47</td>
<td>1.04</td>
<td>1.53</td>
<td>2.08</td>
<td>2.65</td>
</tr>
<tr>
<td></td>
<td>-, -</td>
<td>0.48</td>
<td>1.05</td>
<td>1.60</td>
<td>2.01</td>
<td>2.68</td>
</tr>
<tr>
<td></td>
<td>-, F</td>
<td>0.61</td>
<td>1.41</td>
<td>2.06</td>
<td>2.71</td>
<td>3.75</td>
</tr>
<tr>
<td></td>
<td>F, F</td>
<td>0.75</td>
<td>1.85</td>
<td>2.78</td>
<td>3.89</td>
<td>5.07</td>
</tr>
<tr>
<td></td>
<td>R, R</td>
<td>0.62</td>
<td>1.54</td>
<td>2.39</td>
<td>3.47</td>
<td>4.64</td>
</tr>
<tr>
<td></td>
<td>R, -</td>
<td>0.51</td>
<td>1.15</td>
<td>1.86</td>
<td>2.61</td>
<td>3.57</td>
</tr>
<tr>
<td></td>
<td>R, F</td>
<td>0.38</td>
<td>0.84</td>
<td>1.23</td>
<td>1.72</td>
<td>2.32</td>
</tr>
<tr>
<td></td>
<td>-, -</td>
<td>0.41</td>
<td>0.94</td>
<td>1.32</td>
<td>1.82</td>
<td>2.51</td>
</tr>
<tr>
<td></td>
<td>-, F</td>
<td>0.33</td>
<td>0.72</td>
<td>1.03</td>
<td>1.33</td>
<td>1.75</td>
</tr>
<tr>
<td></td>
<td>F, F</td>
<td>0.30</td>
<td>0.59</td>
<td>0.82</td>
<td>1.09</td>
<td>1.44</td>
</tr>
</tbody>
</table>

**Notes:**
- R: Rise
- F: Fall
- InL: Left Input
- InR: Right Input

Hong-Yi Huang 黃弘一
**Simulation of Interconnect Cross Coupling (0.35 μm)**

<table>
<thead>
<tr>
<th>IN</th>
<th>INL, INR</th>
<th>2000μ m</th>
<th>4000μ m</th>
<th>6000μ m</th>
<th>8000μ m</th>
<th>10000μ m</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Rise (R)</strong></td>
<td>R, R</td>
<td>0.26</td>
<td>0.48</td>
<td>0.76</td>
<td>1.25</td>
<td>1.57</td>
</tr>
<tr>
<td></td>
<td>R, -</td>
<td>0.33</td>
<td>0.64</td>
<td>0.99</td>
<td>1.57</td>
<td>2.06</td>
</tr>
<tr>
<td></td>
<td>R, F</td>
<td>0.43</td>
<td>0.86</td>
<td>1.37</td>
<td>2.07</td>
<td>2.83</td>
</tr>
<tr>
<td></td>
<td>-, -</td>
<td>0.46</td>
<td>0.89</td>
<td>1.43</td>
<td>2.15</td>
<td>2.91</td>
</tr>
<tr>
<td></td>
<td>-, F</td>
<td>0.65</td>
<td>1.32</td>
<td>2.06</td>
<td>3.01</td>
<td>4.28</td>
</tr>
<tr>
<td></td>
<td>F, F</td>
<td>0.90</td>
<td>1.81</td>
<td>2.87</td>
<td>4.11</td>
<td>5.84</td>
</tr>
<tr>
<td><strong>Fall (F)</strong></td>
<td>R, R</td>
<td>0.79</td>
<td>1.73</td>
<td>2.92</td>
<td>4.34</td>
<td>6.19</td>
</tr>
<tr>
<td></td>
<td>R, -</td>
<td>0.54</td>
<td>1.19</td>
<td>2.10</td>
<td>3.12</td>
<td>4.52</td>
</tr>
<tr>
<td></td>
<td>R, F</td>
<td>0.36</td>
<td>0.77</td>
<td>1.29</td>
<td>2.03</td>
<td>2.87</td>
</tr>
<tr>
<td></td>
<td>-, -</td>
<td>0.41</td>
<td>0.86</td>
<td>1.39</td>
<td>2.20</td>
<td>3.13</td>
</tr>
<tr>
<td></td>
<td>-, F</td>
<td>0.31</td>
<td>0.59</td>
<td>0.96</td>
<td>1.56</td>
<td>2.03</td>
</tr>
<tr>
<td></td>
<td>F, F</td>
<td>0.24</td>
<td>0.44</td>
<td>0.75</td>
<td>1.21</td>
<td>1.55</td>
</tr>
</tbody>
</table>

**R**: rise, **F**: fall, **-**: steady
## Simulation of Interconnect Cross Coupling (0.18 um)

<table>
<thead>
<tr>
<th>IN</th>
<th>INL, INR</th>
<th>2000μm</th>
<th>4000μm</th>
<th>6000μm</th>
<th>8000μm</th>
<th>10000μm</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Rise (R)</strong></td>
<td>R, R</td>
<td>2.35</td>
<td>4.66</td>
<td>7.94</td>
<td>1.20</td>
<td>1.72</td>
</tr>
<tr>
<td></td>
<td>R, -</td>
<td>0.30</td>
<td>0.62</td>
<td>1.06</td>
<td>1.69</td>
<td>2.35</td>
</tr>
<tr>
<td></td>
<td>R, F</td>
<td>0.40</td>
<td>0.90</td>
<td>1.58</td>
<td>2.54</td>
<td>3.30</td>
</tr>
<tr>
<td></td>
<td>—, -</td>
<td>0.41</td>
<td>0.95</td>
<td>1.64</td>
<td>2.53</td>
<td>3.77</td>
</tr>
<tr>
<td></td>
<td>—, F</td>
<td>0.63</td>
<td>1.41</td>
<td>2.55</td>
<td>3.96</td>
<td>5.85</td>
</tr>
<tr>
<td></td>
<td>F, F</td>
<td>0.88</td>
<td>1.90</td>
<td>3.37</td>
<td>5.37</td>
<td>7.85</td>
</tr>
<tr>
<td><strong>Fall (F)</strong></td>
<td>R, R</td>
<td>0.73</td>
<td>1.76</td>
<td>3.21</td>
<td>5.10</td>
<td>7.44</td>
</tr>
<tr>
<td></td>
<td>R, -</td>
<td>0.48</td>
<td>1.23</td>
<td>2.25</td>
<td>3.57</td>
<td>5.13</td>
</tr>
<tr>
<td></td>
<td>R, F</td>
<td>0.33</td>
<td>0.72</td>
<td>1.38</td>
<td>2.19</td>
<td>3.24</td>
</tr>
<tr>
<td></td>
<td>—, -</td>
<td>0.36</td>
<td>0.78</td>
<td>1.44</td>
<td>2.19</td>
<td>3.26</td>
</tr>
<tr>
<td></td>
<td>—, F</td>
<td>0.26</td>
<td>0.55</td>
<td>0.98</td>
<td>1.49</td>
<td>2.11</td>
</tr>
<tr>
<td></td>
<td>F, F</td>
<td>0.20</td>
<td>0.41</td>
<td>0.70</td>
<td>1.11</td>
<td>1.58</td>
</tr>
</tbody>
</table>

R: rise, F: fall, -: steady
**Inductance**

- on-chip inductances are normally small
- bond-wire inductance can cause deleterious effects in large, high-speed I/O buffers
- as process shrinks, on-chip inductances might have to be taken into account

**Package inductance** 3nH ~ 15nH
- I noise, ground noise
- voltage change due to transient current spike

\[
dV = L \frac{di}{dt}
\]

It is important to keep the change of internal power supply not to disturb the behavior of the chip.
Case 1 Simulation

<table>
<thead>
<tr>
<th>Case1</th>
<th>△V=最大值-最小值</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1) Out 點之訊號振幅：</td>
<td>2.65v / 2.47v 0.20v / -0.46v △V=0.18v</td>
</tr>
<tr>
<td>邏輯1最大值/邏輯1最小值</td>
<td>△V=0.18v</td>
</tr>
<tr>
<td>邏輯0最大值/邏輯0最小值</td>
<td>△V=0.66v</td>
</tr>
<tr>
<td>(2) Vdd.int 點之訊號振幅 (最大值/最小值)</td>
<td>2.70v / 1.96v 0.65v / -0.29v △V=0.74v</td>
</tr>
<tr>
<td>Gnd.int 點之訊號振幅 (最大值/最小值)</td>
<td>△V=0.94v</td>
</tr>
<tr>
<td>(3) M1(pmos) Current Peak (最大值/最小值)</td>
<td>46.65mA / -4.51mA</td>
</tr>
<tr>
<td>M2(nmos) Current Peak (最大值/最小值)</td>
<td>55.78mA / -17.85mA</td>
</tr>
</tbody>
</table>

Hong-Yi Huang 黃弘一
**Case 2 Simulation**

1. **Out 点之訊號振幅**:
   - 正逻辑 1 最大值 / 逻辑 1 最小值: 3.71v / 1.88v
   - 正逻辑 0 最大值 / 逻辑 0 最小值: 0.89v / -1.49v
   - △V = 1.83v

2. **Vdd.int 点之訊號振幅** (最大值 / 最小值):
   - 3.12v / 1.53v
   - △V = 1.59v

3. **M1(pmos) Current Peak** (最大值 / 最小值):
   - 73.28mA / -36.26mA

4. **M2(nmos) Current Peak** (最大值 / 最小值):
   - 75.21mA / -64.35mA
### Case 3 Simulation

<table>
<thead>
<tr>
<th>Case 3</th>
<th>( \Delta V ) = 最大值-最小值</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1) Out 点之訊號振幅：</td>
<td></td>
</tr>
<tr>
<td>邏輯 1 最大值/邏輯 1 最小值</td>
<td>2.91v / 2.38v</td>
</tr>
<tr>
<td>邏輯 0 最大值/邏輯 0 最小值</td>
<td>0.45v / -0.84v</td>
</tr>
<tr>
<td>(2) Vdd.int 点之訊號振幅 (最大值/最小值)</td>
<td>2.78v / 2.16v</td>
</tr>
<tr>
<td>Gnd.int 点之訊號振幅 (最大值/最小值)</td>
<td>0.36v / -0.46v</td>
</tr>
<tr>
<td>(3) M1(pmos) Current Peak (最大值/最小值)</td>
<td>42.50mA / -9.86mA</td>
</tr>
<tr>
<td>M2(nmos) Current Peak (最大值/最小值)</td>
<td>50.36mA / -24.60mA</td>
</tr>
</tbody>
</table>
Case 4 Simulation

(1) Out 点之信号振幅:
信号 1 最大值/信号 1 最小值
信号 0 最大值/信号 0 最小值
3.41v / 2.10v 0.77v / -1.37v
\( \Delta V = 1.31v \)
\( \Delta V = 2.14v \)

(2) Vdd.int 点之信号振幅 (最大值/最小值)
Gnd.int 点之信号振幅 (最大值/最小值)
3.05v / 1.75v 0.82v / -0.64v
\( \Delta V = 1.30v \)
\( \Delta V = 1.46v \)

(3) M1(pmros) Current Peak (最大值/最小值)
M2(nmos) Current Peak (最大值/最小值)
36.68mA / -14.25mA 42.00mA / -23.60mA
Case 5 Simulation

(1) Out 點之訊號振幅:
   邏輯 1 最大值/邏輯 1 最小值
   邏輯 0 最大值/邏輯 0 最小值
   △V = 2.92v/2.37v
   △V = 0.47v/-0.89v
   △V = 0.55v

(2) Vdd.int 點之訊號振幅 (最大值/最小值)
   △V = 2.80v/1.75v
   △V = 0.82v/-0.54v
   △V = 1.05v
   △V = 1.36v

(3) M1(pmos) Current Peak (最大值/最小值)
   △V = 44.72mA/-10.38mA
   △V = 52.99mA/-25.60mA

<table>
<thead>
<tr>
<th>Case5</th>
<th>△V=最大值-最小值</th>
</tr>
</thead>
<tbody>
<tr>
<td>(1) Out 點之訊號振幅：邏輯 1 最大值/邏輯 1 最小值 邏輯 0 最大值/邏輯 0 最小值</td>
<td>△V=0.55v △V=1.36v</td>
</tr>
<tr>
<td>(2) Vdd.int 點之訊號振幅 (最大值/最小值)</td>
<td>△V=1.05v △V=1.36v</td>
</tr>
<tr>
<td>(3) M1(pmos) Current Peak (最大值/最小值) M2(nmos) Current Peak (最大值/最小值)</td>
<td>△V=44.72mA/-10.38mA △V=52.99mA/-25.60mA</td>
</tr>
</tbody>
</table>
\[ \Delta V = R_1 I_{\text{tot}} + R_1 I_{\text{analog}} + L \frac{dI_{\text{tot}}}{dt} \]
Simulation of Ground Bounce

Vdd,ext : external Vdd
Gnd,ext : external Gnd
Vdd,int : internal Vdd
Gnd,int : internal Gnd

<table>
<thead>
<tr>
<th>Case</th>
<th>L1, L2, L3 (nH)</th>
<th>M1, M2 (um / um)</th>
<th>Input Rise / Fall Time (ns)</th>
<th>CL (pF)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case1</td>
<td>5</td>
<td>200/0.25, 100/0.25</td>
<td>0.5</td>
<td>30</td>
</tr>
<tr>
<td>Case2</td>
<td>10</td>
<td>400/0.25, 200/0.25</td>
<td>0.5</td>
<td>30</td>
</tr>
<tr>
<td>Case3</td>
<td>10</td>
<td>200/0.25, 100/0.25</td>
<td>2</td>
<td>30</td>
</tr>
<tr>
<td>Case4</td>
<td>10</td>
<td>200/0.25, 100/0.25</td>
<td>0.5</td>
<td>10</td>
</tr>
<tr>
<td>Case5</td>
<td>10</td>
<td>200/0.25, 100/0.25</td>
<td>0.5</td>
<td>30</td>
</tr>
</tbody>
</table>
Simulation Model of Multiple Output Drivers/Pads

- number of power/gnd pads
- number of output buffers
- inductor size
- size of output buffer
- slew rate control
- output capacitance
- on-board decoupling capacitance
- on-chip decoupling capacitance
Cascaded Clock Driver and Clock Line Load

Single Driver
- careful global planning
- achieve smallest skew
Clock Buffer

- phase delay
- clock skew
- clock tree synthesizer
- buffer insertion
- adjust line length, line width
- process and power variation
Tree Network Clock Distribution

Identical driver within a given stage
Fanout split into groups
H-Tree Clock Network

Symmetric geometry for clock distribution
Equal RC delay
Final Clock Driver Location of $\alpha$-chip
Noise Sources of Mixed-Signal IC

Substrate Noise
The Noise Coupling Effects

Substrate coupling effects in mixed-signal design
Substrate Model For A Sample Inverter

Substrate model generated with SPACE for A simple inverter
Power Distribution

- IR drop
- electromigration
- ground bounce
- core power supply/gnd, I/O power supply/gnd
- number of power/gnd pins
- noise issues

Mixed analog/digital system
Power Distribution
Chapter 13 Floor Planning of Mixed-Signal IC

- Mixed-Signal IC Floor Plan
- Examples of ADC Floor Plan
- Examples of DAC Floor Plan
Chip Floor Plan Example

- Control
- Memory
- I/O
- Logic Unit
- Clocks
Initial Floorplan

AREA1

AREA2

RAM
Power Distribution
Clock Distribution

Inter-block wide wire

Tributaries inside an area

Clock driver

RAM
Standard-Cell-Based ASIC

- Logic cells caned standard cell library (AND, OR, multiplier, DFF …)
- Pre-designed mega-cells (fully-custom functions, system-level macros, fixed blocks, cores, functional standard blocks)
- All mask layers are customized transistor and interconnect
- Custom blocks can be embedded
Routing Cell-Based IC

- Cell height
- Feed though
- Channel routing
- Power lines
Analog Floorplan & Power Routeplan

- Analog Signal/Power Routing
- Digital Routing
- Analog Signal/Power Routing
- Digital Routing
- Analog Signal/Power Routing
Power Routeplan in Sensitive Channel

Variable Width

AVDD
AVSS
Analog Signal Routing
AVSS
AVDD
Floorplan of Chip

- OP AMPS & CLOCKED SWITCHES
- TRACK-AND-HOLD
- DPGAS AND INTEGRATING CAPACITOR
- DPGA SWITCHES
- PROGRAMING BUS
- DPGA SWITCHES
- DPGAS & INTEGRATING CAPACITORS
- ANALOG ROUTING BETWEEN INTEGRATORS
- OP AMPS & CLOCKED SWITCHES
- SIGNAL OUT
- DECODER
- SIGNAL IN
- CLOCK GENERATOR
Programmable Logic Devices

- No customized mask layers or logic cells
- Fast design turnaround
- A single large block of programmable interconnect
- A matrix of logic macro cells that usually consist of programmable array logic follow by a flip-flop or latch
  - Read Only Memory (ROM), mask ROM
  - Programmable ROM (PROM)
  - Electrical Programmable ROM (EPROM)
  - Electrical Erasable PROM (EEPROM)
Field Programmable Gate Arrays (FPGA)

- None of the mask layers are customized
- A method for programming the basic logic cells and the interconnect
- The core is a regular array of programmable basic logic cells that can implement combinational as well as sequential logic
- A matrix of programmable interconnect surrounds the basic logic cells
- Programmable I/O cells surrounds the core
- Very short design turnaround
Structured Gate Array

- Only interconnection is customized
- Custom blocks embedded (e.g. memory)
PAD Placement

core
Floorplan of the Eight-Order Modulator
Program Counter with Stack Pointer-Chip Floorplan

PC3 Latch  PC2 Latch  PC1 Latch  PC0 Latch  M Latch  INCR Latch

SP3 NOR  SP2 NOR  SP1 NOR  SP0 NOR

D FLIP-Flop  D FLIP-Flop
Master-slave  Master-slave

Combinational circuit

Instruction decoder
RAM Architecture

128x24-Bit Word Array

Pre decoder

Select

Decoder

Select

Pull ups

SENCE

AMPS

PLRs

PLRs
Block Diagram of the ADC
8-Bits 250MHz Per Second ADC Operation Without a Sample & Hold
(a) with separated unit resistor (b) without separated unit resistor
Input Distribution

![Diagram of input distribution]

1. REF
   IN

33. REF
   IN

65. REF
   IN

97

2

34

66

IN 12
8

IN 96

IN 64

IN 32

12
7

95

63
Intermeshed Resistor Reference Ladder

VREF +

Locally Enlarge

VRFL 2
VRFL 1

VRFU 15

Coarse Resistor Ladder

Fine Resistor Ladder

Upper part

Lower part

Switch Array

To Fine Comparator

VREF -
Reference Ladder Configuration in the Second Stage

VREF- VREF+

R1 R64
L1
R30 R35
R31 R34
R32 R33
I1
I2

+ 1 LSB
- +
- 2 LSB

+ 51 LSB
- +
- 62 LSB
- +
- 63 LSB
- +
- 64 LSB
Resistor Network For the Video DAC

- VDD
- Supply ladders for the switches
- Vhigh
- 75
- Supply ladders Coarse ladders
- 125
- Vlow
- Vout
(a) pattern folding of comparator (b) continuous service layout of analog ground & supply voltage line
Basic Current in a DRL Comprising Comparators with Differential Ential-Pair Stages
First-Stage Layout
ADC Floorplan
Analog Preprocessing

Folding amplifier

Sample clock

digital

Sample latch

a b c d e

Analog Vin

V_a V_b V_c V_d V_e

Hong-Yi Huang 黃弘一
Floorplan of Folding and Interpolating Converter Versus Full-parallel Converter
Full-Parallel Flash ADC signals

Comparators

$V_{2^n}$

$V_2$

$V_1$

$V_0$

$V_{in}$

Saturation active saturation

Sample latch

Encoder

$2^n$

$2$

$1$

$0$

Digital output

Clock
12bit Segmented Current-Steering DAC

Binary weighted current source

Unary current cells
Basic Architecture of DAC

63 non-weighted current sources for 6 MSB

Weighted current source for B1 B2 (LSB)

VDD

R_{load (external)}

B8 (MSB) ~ B3

B2, B1 (LSB)
Current Distribution of Current Source

- VDD
- I_{out}
- V_{G1} (Bias voltage)
- Finite resistance of Ground line

Graph showing current distribution with labels:
- GmR = 0
- GmR = 0.01
- GmR = 0.02
- GmR = 0.03
- GmR = 0.04
Two-Step Decoding
High-Speed Decoding Circuit
DAC Architecture

COLUMN DECODER

ROW DECODER

BIT1
BIT0

BINARY WEIGHTED
BINARY WEIGHTED

VREF 1
VREF 2

SW#
SW
Floorplan of the Proposed Segmented DAC Architecture

- **Clock driver**
- **Thermocoder**
  - **Full Decoder**
  - **Latency equaliser**
- **Unary latches & switches**
  - **Swatch Array**
- **Unary current source array**
  - **Current Source Array**

- **VDD**
- **Msw_b**
- **Msw_a**
- **Mcas**
- **Mcur_src**
- **VSS**
- **Un1...255**
- **Bin1...6**
- **255**
- **6**
- **iout**
Circuit Diagram of LSB Cascode Current Source

From Deglitch circuit

M1

M2

M3

M4

Vd

Vd

VB2

VB1

lout (LSB)

lout (LSB)
3.3v-110Mhz 10-bit CMOS Current-Mode DAC

<table>
<thead>
<tr>
<th>H (△) ILSB</th>
<th>G (△) ILSB</th>
</tr>
</thead>
<tbody>
<tr>
<td>40 56 64 48 16 32 24 8 8 32 16 48 64 56 40</td>
<td>52 36 44 60 28 12 4 20 20 4 12 28 60 44 36 52</td>
</tr>
<tr>
<td>59 43 35 51 19 11 27 27 11 19 51 35 43 59</td>
<td>47 63 55 39 7 23 31 15 15 31 23 7 39 55 63 47</td>
</tr>
<tr>
<td>13 29 21 5 37 53 61 45 45 61 53 37 5 21 29 13</td>
<td>25 9 17 49 33 41 57 57 41 33 49 17 9 25</td>
</tr>
<tr>
<td>18 2 10 25 58 42 34 50 50 34 42 58 25 10 2 18</td>
<td>6 22 30 14 46 62 54 38 38 54 62 46 14 30 22 6</td>
</tr>
<tr>
<td>6 22 30 14 46 62 54 38 38 54 62 46 14 30 22 6</td>
<td>18 2 10 25 58 42 34 50 50 34 42 58 25 10 2 18</td>
</tr>
<tr>
<td>25 9 17 49 33 41 57 57 41 33 49 17 9 25</td>
<td>13 29 21 5 37 53 61 45 45 61 53 37 5 21 29 13</td>
</tr>
<tr>
<td>47 63 55 39 7 23 31 15 15 31 23 7 39 55 63 47</td>
<td>59 43 35 51 19 11 27 27 11 19 51 35 43 59</td>
</tr>
<tr>
<td>52 36 44 60 28 12 4 20 20 4 12 28 60 44 36 52</td>
<td>40 56 64 48 16 32 24 8 8 24 32 16 48 64 56 40</td>
</tr>
</tbody>
</table>

Center point
Local matrix
(a) unary current source implemented as one unit (b) as four units in parallel c-as 16 units in parallel
Different Layout Arrangement For the Device M2 and Mc in Each Current Source (4 unit cell & 5 unit cell)
The Proposed Segmented 6+2+4 Current Steering Architecture
# Double Centroid Switching Scheme

![Diagram of Double Centroid Switching Scheme](image)

<table>
<thead>
<tr>
<th>M0</th>
<th>B0</th>
<th>B0</th>
<th>B1</th>
<th>B0</th>
<th>M0</th>
</tr>
</thead>
<tbody>
<tr>
<td>16</td>
<td>14</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>4</td>
<td>2</td>
<td>6</td>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>3</td>
<td>7</td>
<td>7</td>
<td>3</td>
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<tr>
<td>13</td>
<td>15</td>
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</tr>
<tr>
<td>B2</td>
<td>B1</td>
<td>B1</td>
<td>B4</td>
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<tr>
<td>B2</td>
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<td>B1</td>
<td>B4</td>
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<td>5</td>
<td>1</td>
<td>3</td>
<td>8</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
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<td></td>
<td></td>
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<td>5</td>
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<td>13</td>
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<tr>
<td>B2</td>
<td>B1</td>
<td>B1</td>
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<td></td>
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<tr>
<td>13</td>
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<td>8</td>
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<tr>
<td>7</td>
<td>4</td>
<td>2</td>
<td>6</td>
<td></td>
<td></td>
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<td></td>
<td></td>
<td></td>
</tr>
</tbody>
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</tr>
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<td></td>
<td></td>
<td></td>
<td></td>
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<td>4</td>
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<td>6</td>
<td>6</td>
<td>2</td>
</tr>
<tr>
<td>5</td>
<td>1</td>
<td>3</td>
<td>7</td>
<td>7</td>
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<td></td>
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<td>13</td>
<td>15</td>
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<td>5</td>
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<td>3</td>
<td>8</td>
<td></td>
<td></td>
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<td></td>
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<tr>
<td>16</td>
<td>14</td>
<td></td>
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<td></td>
<td></td>
</tr>
</tbody>
</table>
Switching Sequence of Matrix

Column Switching Sequence

<table>
<thead>
<tr>
<th>7</th>
<th>5</th>
<th>3</th>
<th>1</th>
<th>2</th>
<th>4</th>
<th>6</th>
<th>8</th>
</tr>
</thead>
</table>

Current Cell  Ground Line  PAD
Symmetrical Switching

- DEVIATION (POSITIVE)
- DEVIATION (NEGATIVE)
- AVERAGE OUTPUT

CURRENT DISTRIBUTION

LOCATION
1 2 3 4 5 6 7

SEQUENTIAL SWITCHING
6 4 2 1 3 5 7

SYMmetrical SWITCHING
Poly-Diffusion Capacitor with Top-Plate Shield
Unit Capacitor For C-2C Ladder Implementation
Chapter 14  Noise Sources of Mixed-Signal IC

- Modeling And Analysis Of Substrate
- Substrate Noise Effect
- Reduction Substrate Noise
- Analysis of Parasite Effect on Capacitance
- Chip-Package Interface
Parasite Effect on Capacitance

電容模型

$C_p$: 電容和基底形成的寄生電容

$R_{sub}$: 基底的寄生電阻

$C_{sub}$: 基底表面到底層的寄生電容

0.35um 1p4m的MIM電容與基底寄生電容的關係

<table>
<thead>
<tr>
<th></th>
<th>M4 – M3</th>
<th>M3 – M2</th>
<th>M2 – M1</th>
</tr>
</thead>
<tbody>
<tr>
<td>C(pF)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_p$(pF)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C/Cp</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>M4-M3-M2</th>
<th>M4-M3-M2- M1</th>
<th>M4-M3-M2-M1- poly</th>
</tr>
</thead>
<tbody>
<tr>
<td>C(pF)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_p$(pF)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C/Cp</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### 0.35um 2p4m的PIP電容與基底寄生電容的關係

<table>
<thead>
<tr>
<th></th>
<th>poly1 to poly2</th>
</tr>
</thead>
<tbody>
<tr>
<td>C(pF)</td>
<td></td>
</tr>
<tr>
<td>Cp(pF)</td>
<td></td>
</tr>
<tr>
<td>C/Cp</td>
<td></td>
</tr>
</tbody>
</table>

### 0.25um 1p5m的MIM電容與基底寄生電容的關係

<table>
<thead>
<tr>
<th></th>
<th>M5 – M4</th>
<th>M4 – M3</th>
<th>M3 – M2</th>
</tr>
</thead>
<tbody>
<tr>
<td>C(pF)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cp(pF)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C/Cp</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>M2-M1</th>
<th>M5-M4-M3</th>
<th>M5-M4-M3-M2</th>
</tr>
</thead>
<tbody>
<tr>
<td>C(pF)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cp(pF)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>C/Cp</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>M5-M4-M3-M2-M1</th>
<th>M5-M4-M3-M2-M1-poly</th>
</tr>
</thead>
<tbody>
<tr>
<td>C(pF)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Cp(pF)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>C/Cp</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### 0.18um 1p6m的MIM電容與基底寄生電容的關係

<table>
<thead>
<tr>
<th></th>
<th>CTM-M5</th>
<th>CTM-M4</th>
<th>CTM-M3</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>C(pF)</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Cp(pF)</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>C/Cp</strong></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th></th>
<th>CTM-M2</th>
<th>CTM-M1</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>C(pF)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>Cp(pF)</strong></td>
<td></td>
<td></td>
</tr>
<tr>
<td><strong>C/Cp</strong></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Parasite Effect on Resistance

電阻模型

$C_p$: 依電阻佈局方式可以分為$C_{ox}(poly)$、$C_{well}(WELL)$

$R_{sub}$: 基底的寄生電阻

$C_{sub}$: 基底的寄生電容

0.35um poly電阻與基底寄生電容的關係

<table>
<thead>
<tr>
<th></th>
<th>Poly with N+ imp</th>
<th>Poly with P+ imp</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{\square} (\Omega/sq)$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R (\Omega)$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_p (fF)$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Analysis of Substrate Noise
(a) Mixed-Signal Circuit Including the Effect of Substrate Coupling (b) Sideview of Device Layout (c) Signal Waveform
The Layout Used Study Isolation Between Two Contacts / The Equivalent Substrate Model

\[ I = 20 \log \left( \frac{V_{rcv}}{V_{inj}} \right) \]
Isolation In A Low / A High Resistivity Substrate

Distance between contacts (um)
Guard Ring Layout/ Substrate Model / Variation In Isolation As a Function

1000um

W

a b

d

Lgr=8n
Lgr=4n
Lgr=2n
Lgr=0

Isolation (dB)

W(in um)

(inductance of guard ring ground bond-wire)

Hong-Yi Huang 黃弘一
Model of Four Adjacent Tracks (RLC Model)

Vg measured here
The Circuit Configuration Using Active Guard Band Filter

Noise cancellation circuit
Circuit configuration

Noise cancellation circuit
Simplified model
Substrate Coupling Effects In Mixed-Mode ICs

The substrate coupling noise problem
Various Guarding Configurations On Noise Coupling In The Circuit

Effects of various guarding configurations on noise
Power-Supply Noise of Analog/Digital Mixed-Signal IC Design

<table>
<thead>
<tr>
<th></th>
<th>範圍</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{bond}$</td>
<td>小於1 ohm</td>
</tr>
<tr>
<td>$C_{bond}$</td>
<td>1pF〜7pF</td>
</tr>
<tr>
<td>$L_{bond}$</td>
<td>2n〜10nH</td>
</tr>
</tbody>
</table>

範圍：
- $R_{bond}$ 小於1 ohm
- $C_{bond}$ 1pF〜7pF
- $L_{bond}$ 2n〜10nH
Digital oscillator output

Vdd of power-supply noise

Vss of power-supply noise

Amp output noise
Analysis Different Analog Circuit Structure of Power-Supply Noise for Mixed-Signal IC Design

Single end Amp
Gain = 14.2dB, PSRR = 20.8dB
Unity gain frequency = 1.66MHz
R : power line parasitic resister (3 ohm)
L : bonding wire parasitic inductor (10 nH)
Two-stage OP AMP
Gain = 61.9dB 、PSRR = 79.3dB
Unity gain frequency = 1.43MHz
(二)
Folded cascode OP AMP
Gain = 55.9dB 、PSRR = 53.51dB
Unity gain frequency = 1.65MHz

<table>
<thead>
<tr>
<th>Inverter</th>
<th>PMOS</th>
<th>NMOS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Case1</td>
<td>6/0.35</td>
<td>2/0.35</td>
</tr>
<tr>
<td>Case2</td>
<td>24/0.35</td>
<td>8/0.35</td>
</tr>
<tr>
<td>Case3</td>
<td>128/0.35</td>
<td>32/0.35</td>
</tr>
</tbody>
</table>
Different digital noise for power-supply noise

![Graph showing different digital noise for power-supply noise with cases 1, 2, and 3, and different amplifiers: single-end amp, folded-cascode op amp, two-stage op amp.]

Different digital noise for analog output noise

![Graph showing different digital noise for analog output noise with cases 1, 2, and 3, and different amplifiers: single-end amplifier, folded-cascode Op amp, two-stage op amp.]

Hong-Yi Huang 黃弘一
Substrate Noise

VDD

CK

CDB2

M3

M2

RD

VDD

Vin

Vout

Vsub

M1

Distributed Substrate Model

Lb

P-Sub

M2

5v

16k

P+
Substrate Noise

基底模型
The Noise Coupling Effects

Substrate coupling effects in mixed-signal design
Substrate Model For A Sample Inverter

Substrate model generated with SPACE for a simple inverter
### 0.25um poly電阻與基底寄生電容的關係

<table>
<thead>
<tr>
<th></th>
<th>P+ poly w/o silicide</th>
<th>P+ poly w/i silicide</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_{sq}$ (Ω/sq)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R$ (Ω)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_p$ (fF)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R$ (Ω)</td>
<td></td>
<td></td>
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<td>$C_p$ (fF)</td>
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### 0.18um poly電阻與基底寄生電容的關係

<table>
<thead>
<tr>
<th></th>
<th>P+ poly w/o silicide</th>
<th>P+ poly w/i silicide</th>
</tr>
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<tbody>
<tr>
<td>$R_{sq}$ (Ω/sq)</td>
<td></td>
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</tr>
<tr>
<td>$R$ (Ω)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_p$ (fF)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$R$ (Ω)</td>
<td></td>
<td></td>
</tr>
<tr>
<td>$C_p$ (fF)</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Noise in a Sampling Circuit Resulting From the Clock Buffer Supply Bounce
(a) Typical Waveform Observed Experimentally at the Current Source Output  
(b) Typical Output Voltage From Device Simulation

Settling Time to within 0.5mv
Vpp = 8 mv
5.8 ns

Settling Time to within 0.5mv
Vpp = 8 mv
5.8 ns
Connection of Substrate Contact to (a) Analog Ground (b) Digital Ground

(a)

(b)
Conventional Method of Powering up a CMOS Chip in a PGA Package
Circuit Representation of Heavily Doped Substrate

- WELL Contact
- Substrate Contact
- N-WELL
- P+ channel stop implant
- P-Bulk
- Repi1
- Repi2
- Repi3
- Bulk Node

Hong-Yi Huang 黃弘一
Device Simulation Results for Peak-to-Peak Noise As a Function of Distance Between the Digital Noise Source
Lumped Electrical Model of a Chip-Package Interface

Vin

5v

T=1.0ns

1pF

0.1Ω

5nH

(10nH)

Lpin

0.5Ω

0.5pF

100pF

Cvss (1pF)

Lvss (5nH)

0.1Ω
Measure Influence of P+ Guard Rings

Peak-to-Peak Noise mv

Guard Ring Configuration

Dedicated package pin
Connected to large substrate contact

Hong-Yi Huang 黃弘一
Pattern of the Different Ways in which Coupled Devices are Biased
Schematic Illustration of the Package Structure of an Integrated Circuit Showing the Main Parts that Cause Packaging Inductance
Substrate Models Considered (a) Full Model $N(N-1) \div 2$ Resistances (b) $\Pi$ model $2N-1$ Resistances in a Two Dimensional Situation
The LC Parasitic Tank Circuit

VSS PAD
L-C TANK CIRCUIT
VDD PAD
GROUND
METALIZATION
POWER PLANE
The New Method of Applying Power to a CMOS Chip in a PGA Package
Typical Chip-Package Interface Parasitics

- **Internal logic cells**
- **Output driver cell**

**Internal Vss Bus**
- \( i_1 \)

**External Vss Bus**
- \( i_2 \)

**Bonding Parasitics**
- \( L_1 \), \( R_1 \), \( C_1 \), \( R_p \), \( L_p \)

**Pin Parasitics**
- \( L_2 \), \( R_2 \), \( C_2 \), \( C_p \)

**Vss Package Plane**

- \( L_1 \) \( R_1 \) \( C_1 \) : **Bonding Parasitics**
- \( L_2 \) \( R_2 \) \( C_2 \) : **Package Pin Parasitics**
- \( L_p R_p C_p \) : **Vss Plane Parasitics**
Chapter 15 Noise Analysis of Mixed-Signal IC

- Power Supply Noise
- Substrate Noise
- Noise Effect of Parasitic Capacitance
- Noise Effect of Parasitic Resistance
Analysis Different Analog Circuit Structure of Power-Supply Noise

Single end Amp
Gain = 14.2dB、PSRR = 20.8dB
Unity gain frequency = 1.66MHz
R : power line parasitic resister(3 ohm)
L : bonding wire parasitic inductor
(10 nH)
Two-stage OP AMP
Gain = 61.9dB \text{  } PSRR = 79.3dB
Unity gain frequency = 1.43MHz

\( \text{（二）} \)
Folded cascode OP AMP
Gain = 55.9dB 、PSRR = 53.51dB
Unity gain frequency = 1.65MH
(三)
Different Bond Wire L Value for Power-Supply Noise

Different bond wire L value for power-supply noise

- single end amp
- folded cascode op amp
- two-stage op amp

Different bond wire L value (nH)

power-supply noise (mV)

0 2 4 6 8 10 12

0 20 40 60 80 100 120 140

V_{dd}, other signal

L_{bond}, C_{bond}, L_{bond}

V_{dd}, other signal

L_{eff}, C_{eff}, L_{bond}
Different bond wire L value for output noise

Different power line parasitic resistor for analog amp output noise
Digital Noise Frequency for Power-Supply Noise

Digital noise frequency for power-supply noise

- two-stage op amp
- folded cascode op amp

Without digital ckt

digital ckt 55MHz
10MHz
1MHz

unit gain buffer output waveform
Unit Gain Buffer Output Spectrum
(a) Measured Peak-to-Peak Noise as a Function of the Number of Package Pins Used to Bias the Substrate of Circuit Simulation

(b) Measured Noise of Circuit Simulation
(a) Device Simulation Results for Peak-to-Peak Noise as a Function of the Inductance Used to Bias a Backside Substrate Contact (b) Device Simulation Results for Noise Setting Time
Analysis of Substrate Noise
Current Flow Lines in a Lightly Doped Substrate

![Diagram of current flow lines in a lightly doped substrate. The diagram shows the flow of current lines between the substrate contacts, NMOS transistor, and equivalent drain diffusion.]
Substrate Noise and Amplifier Output

Oscillator

Substrate noise

Amplifier output
Different digital noise for substrate noise

![Graph showing different digital noise for substrate noise]

Different digital noise for amp output

![Graph showing different digital noise for amp output]
Frequency Domain

Different digital frequency for substrate noise

Different digital frequency for amp output noise
Amplifier Output Spectrum
CMRR

Two-stage op amp:

\[
A_d = \frac{V_{out}}{V_{id}}
\]

\[
A_{CM} = \frac{V_{out}}{V_{ICM}}
\]

\[
CMRR = \frac{A_d}{A_{CM}}
\]

\[
V_{ICM}^+ = V_{o1} + V_{t2} = V_{dd} - V_{ip2} - \sqrt{\frac{I_{ref}}{2}} \left( \frac{\mu_n C_{ox}}{2} \right) \left( \frac{W}{L} \right)_{p2} + V_{t2}
\]

\[
V_{ICM}^- = V_g + V_{in3} = V_{dd} - V_{ip2} - \sqrt{\frac{I_{ref}}{2}} \left( \frac{\mu_n C_{ox}}{2} \right) \left( \frac{W}{L} \right)_{n2} + V_{t2}
\]
Folded-cascode op amp:

\[
S_5 = \frac{8I_5}{\mu_p C_{ox} V_{SD5}^2}
\]

\[
S_7 = \frac{8I_7}{\mu_p C_{ox} V_{SD7}^2}
\]

\[
V_{ICM}^+ = V_{dd} + \sqrt{\frac{2I_4}{\mu_p C_{ox}}} - V_{t1}
\]

\[
V_{ICM}^- = V_{ss} + \sqrt{\frac{I_3}{\mu_n C_{ox} \left(\frac{W}{L}\right)_1}} + \sqrt{\frac{2I_3}{\mu_n C_{ox}}} + V_{t1}
\]
Noise Effect of Parasitic Capacitance

Switched Capacitor Filter and Substrate Noise

\[ H(s) = \frac{3.302}{S^2 + 1.425S + 1.516} \]

\[ C_4 = \left( \frac{\omega_o}{Q} \right) \frac{T}{Q} = \frac{1}{Q_x} = \frac{C_A}{C_B} \]

\[ C_1 = K_1 \times T = K_1 \frac{1}{\omega_o x} \]

\[ C_2 = C_3 = \omega_o \times T = \frac{1}{x} \]

\[ \begin{align*}
C_4 &= \frac{1}{\omega_o T} \Rightarrow f_o = \frac{f_s}{2\pi x} \n
\end{align*} \]
Frequency Response of Switched Capacitor Filter
**Output Waveform with 20KHz Input**

![Waveform Image]

**Output Waveform with 100KHz Input**

![Waveform Image]
Types of Capacitors

<table>
<thead>
<tr>
<th>Type</th>
<th>Layout</th>
</tr>
</thead>
<tbody>
<tr>
<td>Type1</td>
<td>M4-M3</td>
</tr>
<tr>
<td>Type2</td>
<td>M3-M2</td>
</tr>
<tr>
<td>Type3</td>
<td>M2-M1</td>
</tr>
<tr>
<td>Type4</td>
<td>M4-M3-M2</td>
</tr>
<tr>
<td>Type5</td>
<td>M4-M3-M2-M1</td>
</tr>
<tr>
<td>Type6</td>
<td>M4-M3-M2-M1-poly</td>
</tr>
</tbody>
</table>

Substrate Noise to Switched Capacitor Filter, Types 1-3
Output Drifts of Types 1-6 Capacitors

Substrate Noise of Switched Capacitor Filter

M4-M3

M3-M2

M2-M1
**Substrate Noise v.s. Types 1-6 Capacitors**

- Substrate noise for different capacitance type

**Digital Noise v.s. Substrate Noise of Switched Capacitor Filter**

- Substrate noise for different digital noise
電容器佈局方式以改善基底雜訊:

1. 選擇離基底較遠的材料佈局。
2. 加上guard rings，已隔離雜訊干擾
3. 加上保護層。Ex. N-Well，減少基底雜訊的干擾。
4. 禁止有任何信號線跨過電容器，防止不必要的雜訊耦合。
5. 加大與數位電路的距離，避免數位信號的信號耦合。
6. 電容佈局面積小於100×100 μm²避免天線效應發生。
Noise Effect of Parasitic Resistance

Flash ADC
Substrate Noise

Hong-Yi Huang 黃弘一
若以3位元的ADC，則1 LSB=1/8，1 V_{LSB}=3.3/8

\[ V_{in} \pm V_x = V_{ref}(b_1 \cdot 2^{-1} + b_2 \cdot 2^{-2} + \ldots + b_n \cdot 2^{-n}) \]

\[ V_x = 1/16, \quad R/2 \] 由所造成的為位準偏移

電阻分壓網路中間的用兩個來取代一個R，並在兩個中間接以電容器的原因:

1. 降低傳輸的阻抗，降低傳輸錯誤(transient error)。
2. 將低回復錯誤(recovery error)的產生。
Output of 3-bit Flash ADC

Noise on Resistor String

Voltage Divider

Flash ADC Output Waveform
Substrate Noise of Resistor

Inverter device size

- case1: $M_p=120/0.35$ $M_n=30/0.35$
- case2: $M_p=70/0.35$ $M_n=25/0.35$
- case3: $M_p=24/0.35$ $M_n=8/0.35$

Substrate Noise of Resistor v.s. Digital Noise

R string output noise

Different digital noise
Substrate Noise v.s. Digital Noise

Inverter device size

- **case1**: $M_p=120/0.35$ $M_n=30/0.35$
- **case2**: $M_p=70/0.35$ $M_n=25/0.35$
- **case3**: $M_p=24/0.35$ $M_n=8/0.35$

ADC Output v.s. Digital Noise

Inverter device size

- **case1**: $M_p=120/0.35$ $M_n=30/0.35$
- **case2**: $M_p=70/0.35$ $M_n=25/0.35$
- **case3**: $M_p=24/0.35$ $M_n=8/0.35$
Substrate Resistance v.s. Noise

電阻基底寄生電容大小受基底雜訊影響的關係

substrate noise

case1 : W=10 μm  L=15.13 μm
case2 : W=15 μm  L=22.7 μm
case3 : W=20 μm  L=30.26 μm
Chapter 16 Noise Reduction Techniques of Mixed-Signal IC

- Reduction of Power Supply Noise
- Reduction of Substrate Noise
- Reduction of Noise Induced by Interconnect Resistance
- Reduction of Noise Induced by Interconnect Capacitance
降低電阻雜訊的方法

1. 盡量避免使用 WELL 當電阻，因為 WELL 當電阻會耦合基底雜訊，若是用 WELL 當電阻寬度需大於最小值 5~6 μm，以避免蝕刻時發生增減，阻值也隨之變化。

2. 使用 poly 和 diffusion 當電阻時，在底下加上 WELL 當保護層以隔離基底雜訊，已降低 $C_{sub}$ 的電容值。

3. 使用 poly 當電阻，因為阻值穩定且寄生電容較小受基底雜訊影較小。

4. 加上 guard ring 來降低 $R_{sub}$ 的電阻值，使基底雜訊降低。
Coupling from substrate

- CRITICAL BLOCK
- P+ Guard Ring (GND) clean
- N- Guard Ring (VCC) clean
加大類比和數位佈局時的距離

**Substrate Model**

數位和類比距離對基底雜訊的關係
數位和類比距離對放大器輸出雜訊的關係

distance between analog and digital

<table>
<thead>
<tr>
<th>substrate noise(mV)</th>
<th>distance equal resistor(K ohm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0.9</td>
<td>0</td>
</tr>
<tr>
<td>0.8</td>
<td>20</td>
</tr>
<tr>
<td>0.7</td>
<td>40</td>
</tr>
<tr>
<td>0.6</td>
<td>60</td>
</tr>
<tr>
<td>0.5</td>
<td>80</td>
</tr>
<tr>
<td>0.4</td>
<td>100</td>
</tr>
<tr>
<td>0.3</td>
<td>120</td>
</tr>
<tr>
<td>0.2</td>
<td>140</td>
</tr>
<tr>
<td>0.1</td>
<td>160</td>
</tr>
</tbody>
</table>

**two-stage opamp**

distance between analog and digital equal amp noise

<table>
<thead>
<tr>
<th>amp output noise(mV)</th>
<th>distance equal resistor(K ohm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>60</td>
<td>0</td>
</tr>
<tr>
<td>50</td>
<td>20</td>
</tr>
<tr>
<td>40</td>
<td>40</td>
</tr>
<tr>
<td>30</td>
<td>60</td>
</tr>
<tr>
<td>20</td>
<td>80</td>
</tr>
<tr>
<td>10</td>
<td>100</td>
</tr>
<tr>
<td>0</td>
<td>120</td>
</tr>
</tbody>
</table>

**two-stage opa amp**
separated substrate contacts and guard bonds

Digital switching current

Substrate noise
Far away two signal line shielding

- Line 1
- Line 2
- GND
- Line 1
- GND
- Analog line
- GND
- Digital line
Shielding a Sensitive Line by Lower & Upper Ground Planes
Signal line shielding
Analog & Digital Grounds

Analog Section

La - GNDa

Digital Section

Ld - GNDd
Effect of Supply Noise on (a) a Single-ended Circuit (b) a Differential Circuit
Effect of High-Frequency Supply Noise in Differential Pairs
Reduction of Power-Supply

On chip decoupling capacitance

Decoupling capacitance for power-supply noise

Two-stage OP AMP
Gain = 61.9dB
PSRR = 79.3dB
Unity gain frequency = 1.43MHz
Bonding wire

\[ L_{\text{eff}} = \frac{L_{\text{bond}}}{3} \]

\[ C_{\text{eff}} = 3C_{\text{bond}} \]
差動輸入降低電源雜訊

Power-supply noise

Digital current

降低數位切換暫態電流對電源雜訊的影響

Case 1: Digital
- $M_p = 6/0.35$
- $M_n = 2/0.35$ (藍色)

Case 2: Digital
- $M_p = 24/0.35$
- $M_n = 8/0.35$ (淺藍色)

Case 3: Digital
- $M_p = 128/0.35$
- $M_n = 32/0.35$ (深藍色)

\[
\Delta V = n \Delta i R_{eff} + n L_{eff} \frac{di}{dt}
\]
Use of Multiple Wires to Reduce Overall Inductance
Cross-Sectional View of a Twin-Tub CMOS Chip in a PGA Package Using the Conventional Method of Power Up
Cross-Sectional View of a Twin-Tub CMOS Chip in a PGA Package Using the Substrate Conduction Method
Tapered Ground Line for Reduction of Voltage Drops
(a) Cross-Section Showing P+ Guard Ring Biased Using Dedicated Package Pin  (b) P+ Guard Ring On Chip to Large Substrate Contact
(a) Input Signal Corruption Due to Ground & Substrate Bounce (b) Less Corruption in a Differential Environment
(a) Large Source-Bulk Noise Voltage Due to Separating Substrate Contact Form Analog Ground (b) Suppression of the Effect
Reduction of Substrate Noise

SOI

epitaxial製程
利用guard ring降低基底雜訊

Guard ring對基底雜訊的關係

Guard ring對放大器出雜訊的關係
Distribution of a Reference Voltage for Current Mirror Biasing

Circuit 1
M1

Circuit 2
M2

Circuit n
Mn

Wire Resistance

IREF
MREF
Distribution of Current to Reduce the Effect of Interconnect Resistance
Delay & Dispersion of a Signal in a Long Line

Vin

Vout

TD

Diagram showing a long line with components and a graph illustrating the delay and dispersion of a signal.
Array of Sampling Circuit Sensing an Input
Capacitive Coupling Between Various Lines in a Typical Layout
Reduction of Capacitive Coupling Through the Use of Differential Signaling
CMOS Inverter Driving a Load Capacitance

VDD1
VDD
Ld

lvdd

GND1

Ld

Vout

CL

Hong-Yi Huang 黃弘一
On-Chip Capacitor Used to Lower Supply-Ground Noise Voltage
Addition of On-Chip Bypass Capacitor to Suppress Noise at Node X
Addition of Bypass Capacitor Externally
(a) Corruption of a Signal Due to Coupling
(b) Reduction of Coupling by Differential Operation
Reduction of Coupled Noise by Differential Operation
Reduction of Capacitive Coupling Through the Use of Differential Signaling
Coupling Due to Mutual Inductance Between Wires
Multiple Supply Bond Wires with Mutual Coupling
Reduction of Mutual Coupling by (a) Perpendicular Lines (b) Additional Ground Lines (c) Occasional Ground Lines
Reduction of Mutual Inductance Between Two Wires Carrying Equal & Opposite Currents
(a) Shielding Sensitive Signals by Additional ground lines
(b) Greater Spacing Between Lines to Reduce Coupling
Coupling From Signal Line
Use of Guard Ring to Protect Sensitive Circuit
Chapter 2 Processing

2.1 CMOS PROCESSING

Silicon Wafer

*Czochralski method* – single-crystal method

- starts with a seed of single crystal silicon, and the pull rate and speed of rotation determine the diameter of the crystal rod or ingot
- heavily doped silicon is added to the melt before the single-crystal ingot is pulled
- the ingot is cut into wafers using a large diamond saw
- p⁻ is doped around $N_A \approx 2 \times 10^{21}$ donor/m³, 
  *resistivity* $\approx 10-20 \ \Omega \cdot \text{cm}$.
Epitaxial
The surface of wafer might be doped more heavily, and a single-crystal epitaxial layer of the opposite type might be grown over its surface.
Photolithography

Selected portion of silicon wafer can be masked out so that the same type of processing step can be applied to the remaining areas.

- grow a thin oxide (SiO$_2$) to protect the surface

Fig. 2.1 Selectively hardening a region of photoresist using a glass mask.

*Hong-Yi Huang 黃弘一*
**Photoresist**

- *negative photoresist*, exposed photoresist remains after the masking
- *positive photoresist*, exposed photoresist is dissolved by organic solvents, the photoresist still remains where the mask was opaque
- By using both positive and negative photoresist, a single mask can sometimes be used for two steps.
Fig. 2.2 Forming an n well by diffusing phosphorus from a gas into the silicon, through the opening in the SiO₂
- Dopant is Phosphorus for n-well, Arsenic takes much longer time to diffuse.
- 900-1100 °C, high temperature causes dopant to diffuse vertically and laterally. Dopant concentration is the greatest at surface.
- **Boron** for p-well.
Ion implementation

Fig. 2.3 An ion-implantation system
- Allows more independent control over concentration and the thickness of doped region.
- Ion beams are focused and accelerated at 10 keV and 1 MeV.
- Lattice damage due to nuclear collisions results in displacement of substrate atoms.
- Narrow profile results in heavy concentration (Arsenic with 100 keV, 0.06 um ± 0.02 um.)
- Greater control over doping level.
- Much smaller side wall diffusion, allows devices to be more closely spaced, minimize overlap between gate-source and gate-drain regions.
Annealing

Fig. 2.4 Dopant profiles after ion implantation both before and after annealing

- 1000 °C for 15-30 minutes, then cooled down.
- Broaden concentration profile, make profile more uniform.
- Solve the above mentioned problems in ion implementation.
Chemical Vapor Deposition
- E.g. Si$_3$N$_4$ deposited during a gas-phase reaction at about 800 ºC.

Field-implementation

Fig. 2.5 The cross section when field-implants are being formed
- Field implant where field-oxide grown.
- Guarantee silicon under field-oxide will never invert when the conductor over the field-oxide has a large voltage.
- Leakage between junctions of separate transistors in the substrate region is intended to be unconnected.
Growing Field-Oxide: *thermal oxide*

**Wet process:** water vapor diffuses into silicon

\[
\text{Si} + 2\text{H}_2\text{O} \rightarrow \text{SiO}_2 + 2\text{H}_2
\]

**Dry process:** oxygen introduced over wafer, slightly higher temperature than wet process

\[
\text{Si} + \text{O}_2 \rightarrow \text{SiO}_2
\]

Fig. 2.6 The cross section after the field-oxide has been grown.
- SiO₂ takes up approximately 2.2 times the volume of the original silicon, causes SiO₂ to extend approximately 45 percent into, and 55 percent above the surface.
- Wet process is faster because H₂O diffuses faster in silicon than O₂ does.
- Dry process results in denser, higher-quality SiO₂ that is less porous.
Gate-Oxide and Threshold-Voltage Adjust

Fig. 2.7 Cross section after the thin gate-oxide growth and threshold-adjust implant.
- After gate-oxide (about 0.01-0.03 um) is grown, donors (boron) are implemented through the oxide to adjust the threshold voltage.
- p-transistor and n-transistor are adjusted at the same time (n-transistor from -0.1 to 0.7-0.8, p-transistor from -1.6 to -0.8-0.9.
- Higher doping level increases the junction capacitance and body effect of transistors in the well.
- Double threshold adjust allows optimum well doping.
Polysilicon Gate Formation

Fig. 2.8 Cross section after depositing and patterning the polysilicon gates.

- Chemical deposition of polysilicon with silane (SiH₄) gas.
- 650 °C, noncrystalline or amorphous. (1000-1250 °C on silicon to create single-crystal silicon)
- Ion implemented with Arsenic to increase its conductivity (10-30 Ω/□)
Implanting Junction

Fig. 2.9 Cross section after ion-implanting the p⁺ junctions.
Fig. 2.10 Cross section after ion-implanting the n⁺ junctions.
- Boron implemented to from p+ region. self-aligned to poly edge, resulting in very little overlap.
- p+ also for substrate Vss contact to prevent latch-up.
- Arsenic implemented to from n+ region.
- N+ also for n-well V\textsubscript{DD} contact to prevent latch-up.
- After all junctions have been implanted, the complete wafer is covered in CVD SiO\textsubscript{2}. 500 °C, 0.25-0.5 um.
- Next step, open contact hole.
Depositing and Patterning Metal

- Aluminum ( Al ) for interconnection
- *Evaporation* techniques in a vacuum, the heat for evaporation is produced by electron-beam bombarding in a sputtering system.
- Low-temperature annealing ( 550ºC ), give better bonds between metal and silicon.
**Overglass Deposition**

Final *passivation* CVD SiO₂ is deposited, often an additional Si₃N₄ is deposited for better impervious to moisture.

*Fig. 2.11* Final cross section of an example CMOS microcircuit.
Some possible process:
- twin wells
- poly-poly capacitor, thin thermal oxide
- high resistivity poly, 1G Ω/□, SRAM
- field-implant under field-oxide in well region
- n-channel and p-channel transistors with different threshold adjust
- 2, 3, 4, 5, or 6 layer of metal
- planarized after each metal-patterning step, reactive etching, cover with SiO₂, the hills are etched faster than the valleys
- thin-film nichrome resistors under the top layer of metal
- transistors realized in epitaxial layer
- BiCMOS
2.2 BIPOLAR PROCESSING

Fig. 2.12 Cross section of a modern, self-aligned bipolar transistor with oxide isolation. The term “poly” refers to polysilicon.
- p⁻ substrate
- n⁺ region to lower series collector resistance
- n⁻ single-crystal epitaxial
- n⁺ collector contact region is implemented, the region extends from surface down to n⁺ buried region
- polysilicon is used to contact emitter, base, collector
- base p⁺ polysilicon is deposited first, during a high temperature step, the boron dopant from polysilicon contact diffuses into silicon to make underlying region p⁺.
- base polysilicon is covered with a thin layer of SiO₂ (0.5um in thickness), the SiO₂ spacer allows the base contact, thereby minimizing base resistance.
- n⁺ from emitter polysilicon diffuses into the base p silicon to form emitter region.
2.3 INTEGRATION
N-WELL CMOS TECHNOLOGY

(a)
Figure 1: Well implant and drive-in in the n-well CMOS inverter. Window in the mask (a) and cross-section (b)
N-WELL CMOS TECHNOLOGY

(a)

field oxide
Figure 2: Formation of the active regions in the n-well CMOS inverter. Window in the mask (a) and cross-section of the inverter (b).
N-WELL CMOS TECHNOLOGY

(a)
Figure 3: Active regions in the n-well CMOS inverter. Edges of active regions in the mask (a) and cross-section of the inverter.
N-WELL CMOS TECHNOLOGY
(a)
Figure 4: Gate oxide growth in the n-well CMOS inverter. Edges of the gate oxide regions (a) and cross-section of the inverter (b).
N-WELL CMOS TECHNOLOGY

CVD: usually doped with n-type impurity with low resistivity

(a)
Figure 5: Polysilicon region in the n-well CMOS inverter. Window in the mask (a) and cross-section of the inverter (b).
N-WELL CMOS TECHNOLOGY

(a)
Figure 6: Implantation of n-channel transistor drain and source. Window in the n-select mask (a) and cross-section of the inverter (b).
N-WELL CMOS TECHNOLOGY
(a)
Figure 7: Implantation of $p^+$ regions. Window in the negative of the n-select mask (a) and cross-section of the inverter (b).
N-WELL CMOS TECHNOLOGY

(a)
Source/drain annealing at a shoot thermal process to repair some of the crystal structure change occur in the high-close implantation without significant lateral diffusion.

Figure 8: N⁺ region in the n-well of the CMOS inverter. Edges of the drain region of the p-channel device and the n⁺ region in the n-well (a) and cross-section of the inverter (b).
N-WELL CMOS TECHNOLOGY

(a)
The nonplanarity of ton surface will have an impact on the metal deposition step

Figure 9: CVD deposition of SiO$_2$ in the n-well CMOS process. Layout (a) and cross-section of the inverter (b)
N-WELL CMOS TECHNOLOGY
- in the source/drain areas or poly layers.
- contacts to poly must be made outside the gate region to avoid metal spikes through the poly and the thin gate oxide.

(a)
Figure 10: Contact cuts in the n-well CMOS inverter. Window in the mask (a) and cross-section of the inverter (b).
N-WELL CMOS TECHNOLOGY

- “Al” deposited over the entries wafer
- Step coverage is the most critical.
- undefined Al is removed.

(a)
Figure 11: Metallization in the n–well CMOS inverter. Window in the mask (a) and cross-section of the inverter (b).
N-WELL CMOS TECHNOLOGY

Final step: passivation glass to protect the surface from contaminants and scratches.

(a)
Figure 12: CMOS inverter. Composite layout (a), cross-section (b), and electrical diagram (c).
THE SILICON GATE N-CHANNEL TECHNOLOGY

LDD allow very small transistor without suffering from "hot electron"

(a)

(b)
Figure 13: Formation of the LDD transistor structure
THE ADVANCED TWIN-TUB CMOS PROCESS

twin-well
- allows independent control of the threshold voltage.
- keeps resistivity of the wells small.

(a)
Figure 14: Advanced CMOS process. Part 1.

during the steps, both P-well and n-well are rediffused deeper.
THE ADVANCED TWIN-TUB CMOS PROCESS

(a)  

(b)
Figure 15: Advanced CMOS process. Part 2.
THE ADVANCED TWIN-TUB CMOS PROCESS

(a)

(b)
due to the large diffusivity of Boron, the edge of the p-channel are moving jauter than the edges of the n-transistor

Figure 16: Advanced CMOS process. Part 3.
THE ADVANCED TWIN-TUB CMOS PROCESS

(a)

(b)

first metal

or Alloys of Al, Mo, and W
Figure 17: Advanced CMOS process. Part 4.
THE ADVANCED TWIN-TUB CMOS PROCESS
etched with a solution that has the same etching rate for photoresistor & oxide

(a)
Figure 18: Advanced CMOS process. Part 5.
THE ADVANCED TWIN-TUB CMOS PROCESS

- two layer method, high quality due to planrization step
- LDD:NMOS preventing hot-electron phonemena
- optimal threshold voltage both PMOS & NMOS through twin-well
- good latch-up protection by minimizing, the lateral voltage drops inside the wells
Figure 19: The Advanced CMOS process. Summary of basic features.