IEE 5710 Data-Conversion Integrated Circuits

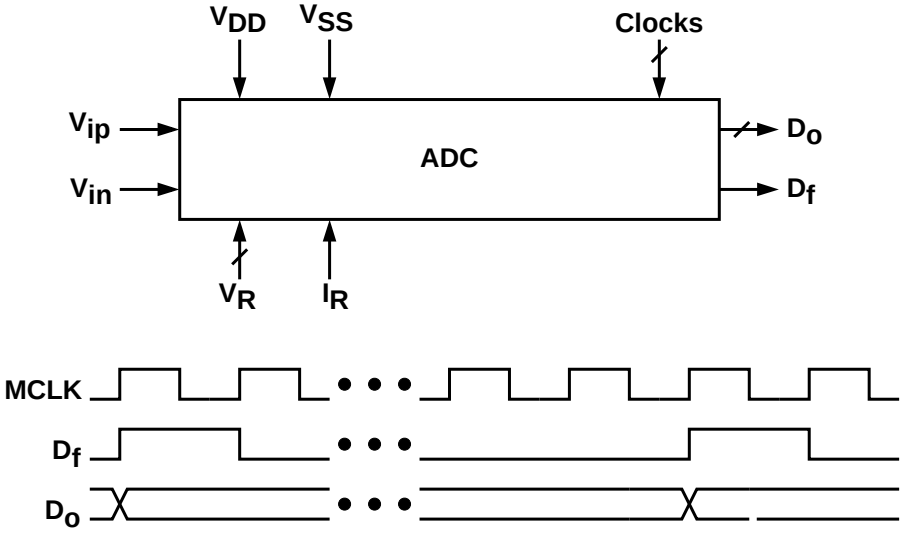
Project 3

You are to design a 1 MS/s 10-bit analog-to-digital converter using the CIC 0.18 μm CMOS technology. The ADC interface is shown below. The analog inputs, V_{ip} and V_{in}, have a differential voltage range of ±0.8 V, and a common-mode voltage of 0.9 V. The corresponding 10-bit digital output is D_o. Another digital output D_f indicates the ADC operation status. The analog input is sampled during $D_f = 1$. The digital output D_o is updated when $D_f = 1$ changes from 0 to 1.

Beside V_{DD} and V_{SS}, you may need several external reference voltages, V_R, to provide ADC references and common-mode voltages. An external reference current can be provided to bias analog circuits. External multi-phase clocks and their variations are also available.

The ADC specifications are:

Maximum Sampling Rate	1 MS/s
Resolution	10 Bits
Input voltage range	±0.8 V
DNL	±0.5 LSB
INL	±0.5 LSB
SNDR	> 55 dB for f_{in} up to 500 kHz
SFDR	> 65 dB for f_{in} up to 500 kHz
Power dissipation	Minimum
Supply voltage	1.8 V
Temperature	



The followings are guidelines:

1. Let V_{DD} = 1.8 V and V_{SS} = 0 V.
2. No need to design clock generator. The external clocks can be modeled using signal sources in SPICE. However, CMOS inverters must be inserted between signal sources and ADC.
3. External voltage references can be modeled using voltage sources in series with 1 kΩ resistors.
4. A temperature of 50˚C is assumed.
5. You are required to minimize the circuit's power consumption while achieving the required specifications.

Homework 6

1. Design the capacitor array and analog switches. State your design considerations.
2. Estimate the specifications of the comparator.
3. Design the digital logic to operate the ADC.
4. To verify your system-level design, simulate the ADC with comparator macro model.
5. Turn in a design and simulation summary. DO NOT turn in the raw SPICE print out.

Homework 7

1. Design the comparator. State your design considerations.
2. Carefully choose the W and L for all devices for minimize power dissipation. State your design considerations.
3. The comparator must past the overdrive recovery test. In the first comparsion cycle, the comparator input is $+V_R$. Then in the next cycle, the comparator must be able to resolve $\pm\Delta/4$.
4. Do Monte Carlo simulation to extract the statistics of the comparator's input-referred offset, V_{OS}.
5. Turn in a design and simulation summary. DO NOT turn in the raw SPICE print out.

Homework 8

1. Simulate the ADC with the comparator you have designed.
2. If the ADC cannot meet the specifications, you have to figure out why, and modified your design accordingly.
3. Your final report should include all design considerations and simulation results, and should be written in the format of a IEEE JSSC paper, such as this example. A paper template can be found here. The report can be written in Chinese or English. Plagiarism is forbidden, even from listed references.